42V Quad Monolithic Synchronous Step-Down Regulator

FEATURES

- **Flexible Power Supply System Providing Four Outputs with a Wide Input Range**
- **Two High Voltage Synchronous Buck Regulators:**
  - **3V to 42V Input Voltage Range**
  - **Output Currents Up to 2.5A and 1.5A**
  - **High Efficiency Up to 93%**
- **Two Low Voltage Synchronous Buck Regulators:**
  - **2.6V to 5.5V Input Voltage Range**
  - **Output Currents Up to 1.8A and 94% Efficiency**
- **Resistor Programmable and Synchronizable 250kHz to 2.2MHz Switching Frequency**
- **Low Ripple Burst Mode® Operation:**
  - **30µA I_Q at 12V_{IN}**
  - **Output Ripple < 15mV**
- **Programmable Power-On Reset**
- Power Good Indicators
- 2-Phase Clock Reduces Input Current Ripple
- Available in Thermally Enhanced 40-Lead QFN (6mm × 6mm) or 48-Lead (7mm × 7mm) LQFP Packages
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive Systems
- Distributed Supply Regulation
- Industrial Controls and Power Supplies

DESCRIPTION

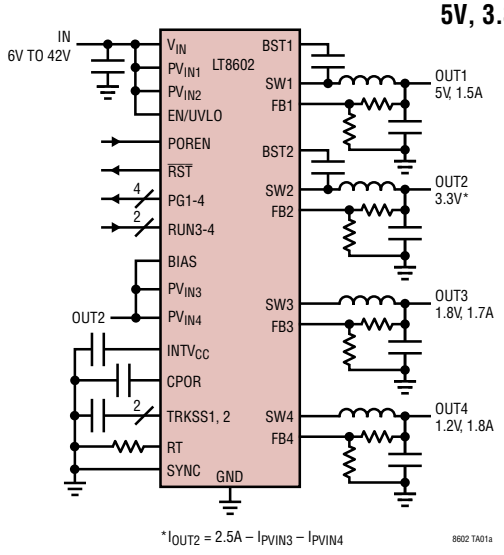
The LT®8602 is a quad channel, current mode, monolithic buck switching regulator with a programmable power-on reset. All regulators are synchronized to a single oscillator with an adjustable frequency from 250kHz to 2.2MHz. The LT8602 can be configured for micropower Burst Mode operation or pulse-skipping operation at light load. Micropower operation results in quiescent current of 30µA with all four regulators operating in the application below.

The high voltage channels are synchronous buck regulators that operate from an input of 3V to 42V. The output currents are up to 1.5A (OUT1) and 2.5A (OUT2). The low voltage channels operate from an input of 2.6V to 5.5V. Internal synchronous power switches provide high efficiency with output currents up to 1.8A. The LT8602 uses a 2-phase clock with channels 1 and 3 operating 180° from channels 2 and 4 to reduce input ripple current on both HV and LV inputs. All channels have cycle-by-cycle current limit, providing protection against shorted outputs. Thermal shutdown provides additional protection.

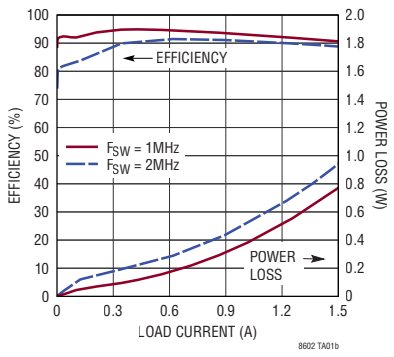
The LT8602 is available in either a 40-lead 6mm × 6mm QFN or a 48-Lead 7mm × 7mm LQFP package.

TYPICAL APPLICATION

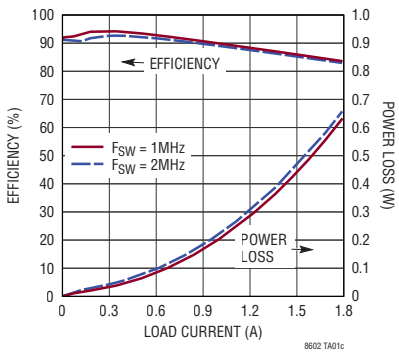
5V, 3.3V, 1.8V and 1.2V Step-Down Regulators



HV Channel Efficiency, V_{IN} = 12V, V_{OUT1} = 5V



LV Channel Efficiency, V_{OUT3} = 1.8V



Rev. C

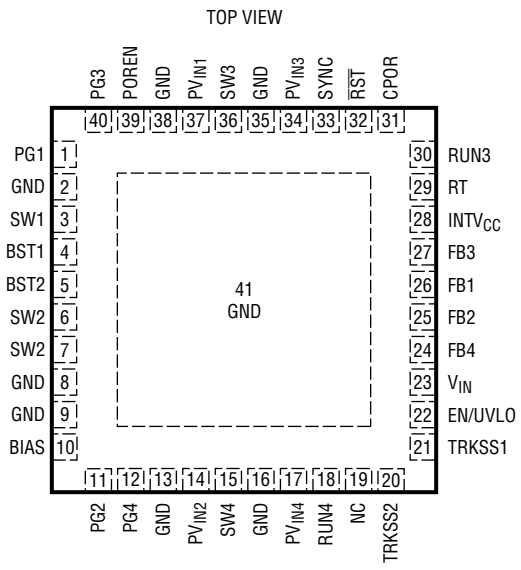
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltages
- V_{IN}, $PV_{IN1,2}$ ..... –0.3V to 42V
- $PV_{IN3,4}$ ..... –0.3V to 6V

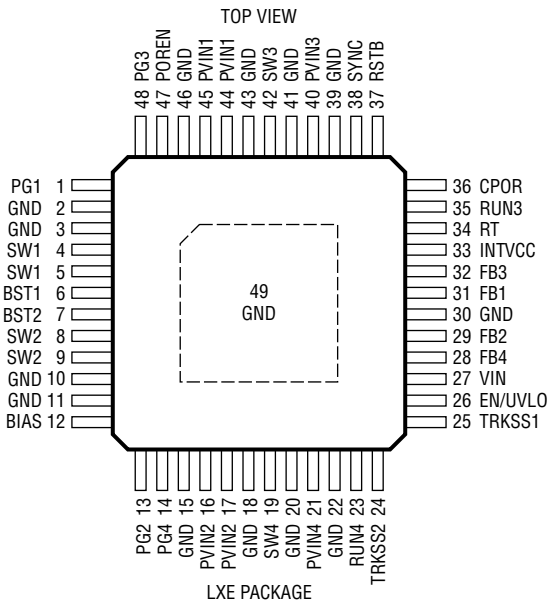
PG1-4, SYNC, TRKSS1-2, RUN3-4, $\overline{RST}$ Voltages 6V
RT, FB1-4, CPOR, POREN Voltages 3.6V
EN/UVLO Voltage 42V
BIAS Voltage ..... –0.3V to 15V
Operating Junction Temperature (Notes 2, 3)
- LT8602E ..... –40°C to 125°C
- LT8602I ..... –40°C to 125°C
- LT8602J ..... –40°C to 150°C

Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN
θ_{JC} = 2°C/W, θ_{JA} = 33°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB



LXE PACKAGE
48-LEAD (7mm × 7mm) PLASTIC LQFP
θ_{JA} = 20°C/W
EXPOSED PAD (PIN 49) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL (QFN)/ TRAY (LXE)	PART MARKING*	PACKAGE DESCRIPTION	MSL RATING	TEMPERATURE RANGE
LT8602EUJ#PBF	LT8602EUJ#TRPBF	LT8602UJ	40-Lead (6mm × 6mm) Plastic QFN	1	–40°C to 125°C
LT8602IUJ#PBF	LT8602IUJ#TRPBF	LT8602UJ	40-Lead (6mm × 6mm) Plastic QFN	1	–40°C to 125°C
LT8602JUJ#PBF	LT8602JUJ#TRPBF	LT8602UJ	40-Lead (6mm × 6mm) Plastic QFN	1	–40°C to 150°C
LT8602ELXE#PBF	LT8602ELXE#TRPBF	LT8602LXE	48-Lead (7mm × 7mm) Plastic eLQFP	3	–40°C to 125°C
LT8602ILXE#PBF	LT8602ILXE#TRPBF	LT8602LXE	48-Lead (7mm × 7mm) Plastic eLQFP	3	–40°C to 125°C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL (QFN)/ TRAY (LXE)	PART MARKING*	PACKAGE DESCRIPTION	MSL RATING	TEMPERATURE RANGE
AUTOMOTIVE PRODUCTS**					
LT8602EUJ#WPBF	LT8602EUJ#WTRPBF	LT8602UJ	40-Lead (6mm × 6mm) Plastic QFN	1	–40°C to 125°C
LT8602IUJ#WPBF	LT8602IUJ#WTRPBF	LT8602UJ	40-Lead (6mm × 6mm) Plastic QFN	1	–40°C to 125°C
LT8602JUJ#WPBF	LT8602JUJ#WTRPBF	LT8602UJ	40-Lead (6mm × 6mm) Plastic QFN	1	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V, PV_{IN3} = PV_{IN4} = 3.3V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operating Voltage		●		2.7	3	V
Minimum Operating Voltage, to Start		●		3.1	3.5	V
V_{IN} Quiescent Current, Shutdown	EN/UVLO = 0.4V			0.1	1	µA
V_{IN} Quiescent Current, Operating	No Load (Note 4) 100µA on V_{OUT2} (Note 4)			30 70		µA µA
EN/UVLO Threshold	EN/UVLO Rising		1.15	1.2	1.25	V
EN/UVLO Hysteresis				50		mV
EN/UVLO Input Current	EN/UVLO = 2V		–40		40	nA
Oscillator						
Switching Frequency	R_T = 28.9k, E-, I-Grade R_T = 28.9k, J-Grade R_T = 254k, E-, I-Grade R_T = 254k, J-Grade	● ● ● ●	1.8 1.75 0.225 0.224	2 2 0.25 0.25	2.2 2.2 0.275 0.284	MHz MHz MHz MHz
SYNC Input Frequency Range		●	0.25		2.2	MHz
SYNC Input Voltage Low		●			0.3	V
SYNC Input Voltage High		●	1.2			V
SYNC Input Current			–100		100	nA
Channel 1						
Feedback Voltage FB1	E-, I-Grade J-Grade	● ●	0.988 0.98	1 1	1.012 1.015	V V
FB Voltage Line Regulation	V_{IN} = 3V to 42V			0.002	0.01	%/V
Input Current FB1		●	–100		100	nA
SW1 Peak Current Limit	V_{IN} = P_{VIN1} = 6V		2.3	2.7	3.0	A
SW1 Leakage Current				0.1	1	µA
SW1 Top On Resistance	I_{SW1} = 1A			240		mΩ
SW1 Bottom On Resistance	I_{SW1} = 1A			170		mΩ
Lower FB1 Power Good Threshold	Percentage of V_{FB1}	●	89	92	95	%
Upper FB1 Power Good Threshold	Percentage of V_{FB1}	●	105	108	111	%
PG1 Output Voltage Low	I_{PG1} = –100µA	●		0.1	0.2	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V, PV_{IN3} = PV_{IN4} = 3.3V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PG1 Leakage Current	PG1 = 5V, FB1 = 1V	●			30	µA
TRKSS1 Pull-Up Current	SS1 = 0.2V		1.5	2.4	3.1	µA
Minimum Switch-On Time	I_{SW1} = 1A			60		ns
Minimum Switch-Off Time	I_{SW1} = 1A			70		ns
Channel 2						
Feedback Voltage FB2	E-, I-Grade J-Grade	● ●	0.988 0.98	1 1	1.012 1.015	V V
FB Voltage Line Regulation	V_{IN} = 3V to 42V			0.002	0.01	%/V
Input Current FB2		●	–100		100	nA
SW2 Peak Current Limit	V_{IN} = P_{VIN2} = 6V		3.5	4.0	4.5	A
SW2 Leakage Current				0.1	1	µA
SW2 Top On Resistance	I_{SW2} = 1A			150		mΩ
SW2 Bottom On Resistance	I_{SW2} = 1A			100		mΩ
Lower FB2 Power Good Threshold	Percentage of V_{FB2}	●	89	92	95	%
Upper FB2 Power Good Threshold	Percentage of V_{FB2}	●	105	108	111	%
PG2 Output Voltage Low	I_{PG2} = –100µA	●		0.1	0.2	V
PG2 Leakage Current	PG2 = 5V, FB2 = 1V	●			30	µA
TRKSS2 Pull-Up Current	SS2 = 0.2V		1.5	2.4	3.1	µA
Minimum Switch-On Time	I_{SW2} = 2A			60		ns
Minimum Switch-Off Time	I_{SW2} = 2A			70		ns
Channel 3						
Operating Voltage		●	2.6		5.5	V
Feedback Voltage FB3	E-, I-Grade J-Grade	● ●	790 784	800 800	810 812	mV mV
FB Voltage Line Regulation	V_{IN} = 3V to 42V			0.002	0.01	%/V
Input Current FB3		●	–100		100	nA
SW3 Average Current Limit			1.8	3.1	3.5	A
SW3 Leakage	PV_{IN3} = 5.5V			0.1	1	µA
SW3 PMOS On Resistance	I_{SW3} = 1A			150		mΩ
SW3 NMOS On Resistance	I_{SW3} = 1A			120		mΩ
Lower FB3 Power Good Threshold	Percentage of V_{FB3}	●	89	92	95	%
Upper FB3 Power Good Threshold	Percentage of V_{FB3}	●	105	108	111	%
PG3 Output Voltage Low	I_{PG3} = –100µA	●		0.1	0.2	V
PG3 Leakage Current	PG3 = 5V, FB3 = 0.8V	●			30	µA
RUN3 Threshold Voltage	200mV/ms Falling Ramp	●	0.695	0.72	0.75	V
RUN3 Input Current	RUN3 = 3.3V	●	–100		100	nA
Soft-Start Time		●	0.7	1	1.3	ms
Minimum Switch-On Time	I_{SW3} = 1A			70		ns
Minimum Switch-Off Time	I_{SW3} = 1A			70		ns
PV_{IN3} UVLO				2.35	2.6	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V, PV_{IN3} = PV_{IN4} = 3.3V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Channel 4						
Operating Voltage		●	2.6		5.5	V
Feedback Voltage FB4	E-, I-Grade J-Grade	● ●	790 784	800 800	810 812	mV mV
FB Voltage Line Regulation	V_{IN} = 3V to 42V			0.002	0.01	%/V
Input Current FB4		●	–100		100	nA
SW4 Average Current Limit			1.8	3.1	3.5	A
SW4 Leakage	PV_{IN4} = 5.5V			0.1	1	µA
SW4 PMOS On Resistance	I_{SW4} = 1A			150		mΩ
SW4 NMOS On Resistance	I_{SW4} = 1A			120		mΩ
Lower FB4 Power Good Threshold	Percentage of V_{FB4}	●	89	92	95	%
Upper FB4 Power Good Threshold	Percentage of V_{FB4}	●	105	108	111	%
PG4 Output Voltage Low	I_{PG4} = –100µA	●		0.1	0.2	V
PG4 Leakage Current	PG4 = 5V, FB4 = 0.8V	●			30	µA
RUN4 Threshold Voltage	200mV/ms Falling Ramp	●	0.695	0.72	0.75	V
RUN4 Input Current	RUN4 = 3.3V	●	–100		100	nA
Soft-Start Time		●	0.7	1	1.3	ms
Minimum Switch-On Time	I_{SW4} = 1A			70		ns
Minimum Switch-Off Time	I_{SW4} = 1A			70		ns
PV_{IN4} UVLO				2.35	2.6	V
Power-On Reset						
CPOR Pull-Up Current	CPOR = 0V			2		µA
POR Delay Time	CPOR = 1000pF		31	35.2	39.4	ms
$\overline{RST}$ Output Voltage Low	$I_{\overline{RST}}$ = –100µA	●		0.1	0.2	V
$\overline{RST}$ Pull-Up Current	POR Timed Out, $\overline{RST}$ = 0V			20		µA
$\overline{RST}$ Leakage Current	$\overline{RST}$ = 6V, EN/UVLO = 0V		–40		40	nA
POREN Threshold		●	1.15	1.2	1.25	V
POREN Pull-Up Current	POREN = 0V		0.8	1.2	1.6	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8602E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8602I is guaranteed to meet performance specifications from –40°C to 125°C junction temperature. The LT8602J is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures above 125°C.

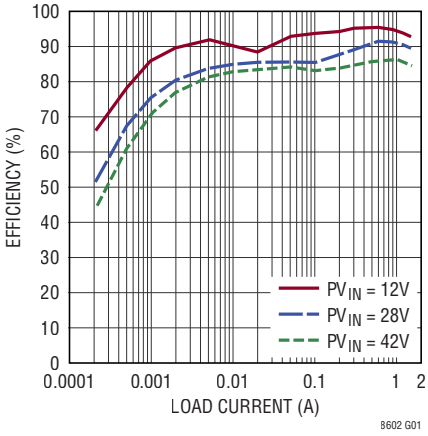
Note 3: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

Note 4: All four channels enabled as shown in the application circuit details of front page application (using the 1MHz component values) found in the Typical Application section.

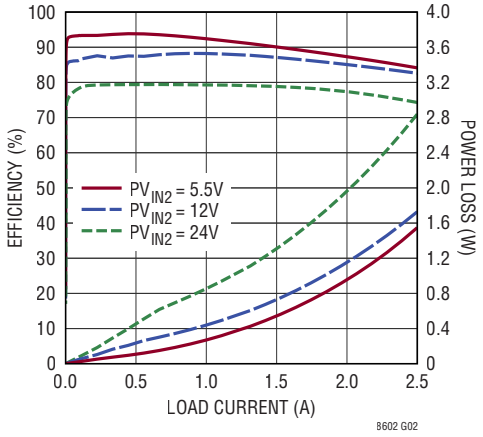
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V and PV_{IN3} = PV_{IN4} = 3.3V, unless otherwise noted.

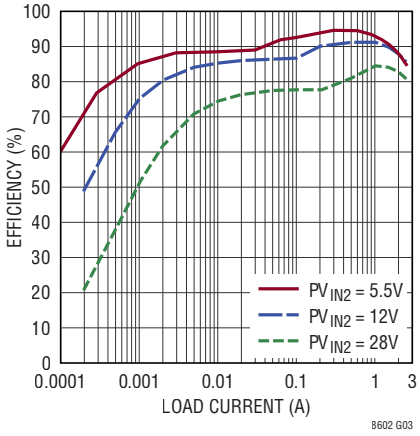
Channel 1 Efficiency vs Load
V_{OUT1} = 8V, f_{SW} = 2MHz



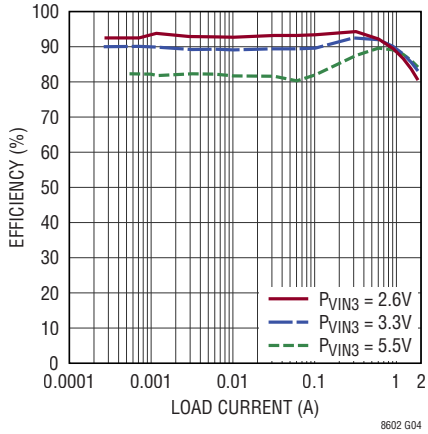
Channel 2 Efficiency vs Load
V_{OUT2} = 3.3V, f_{SW} = 2MHz



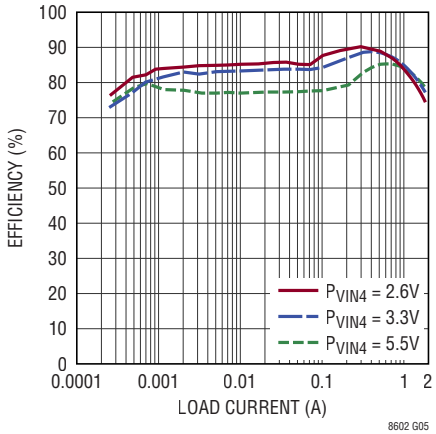
Channel 2 Efficiency vs Load
V_{OUT2} = 3.3V, f_{SW} = 1MHz



LV Channel Efficiency vs Load
V_{OUT3} = 1.8V, f_{SW} = 1MHz



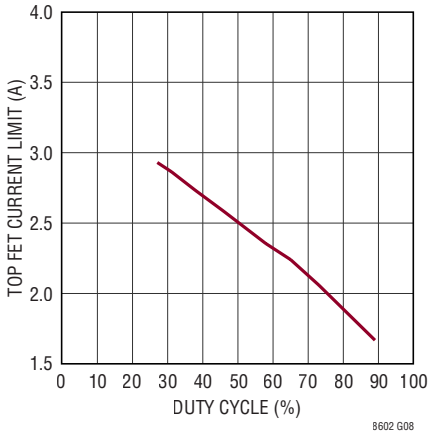
LV Channel Efficiency vs Load
V_{OUT4} = 1.2V, f_{SW} = 2MHz



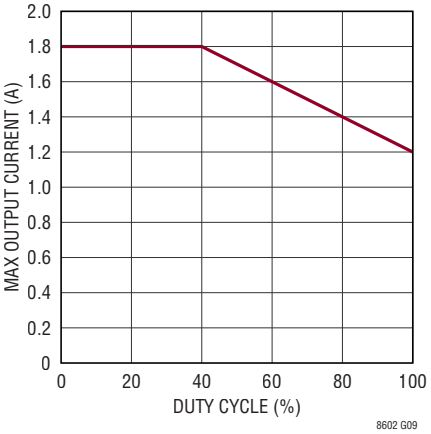
Channel 1 Peak Current Limit vs Duty Cycle

Channel 2 Peak Current Limit vs Duty Cycle

Channel 3/4 Peak Current Limit vs Duty Cycle



Channel 3/Channel 4 Maximum Output Current vs Duty Cycle

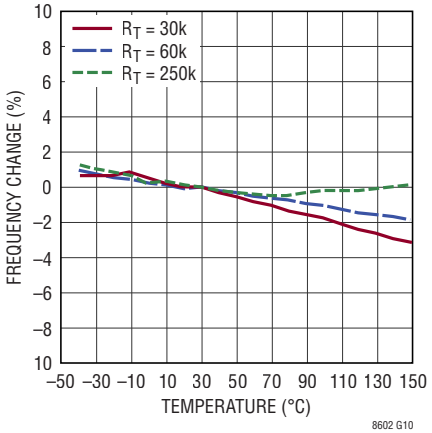


Rev. C

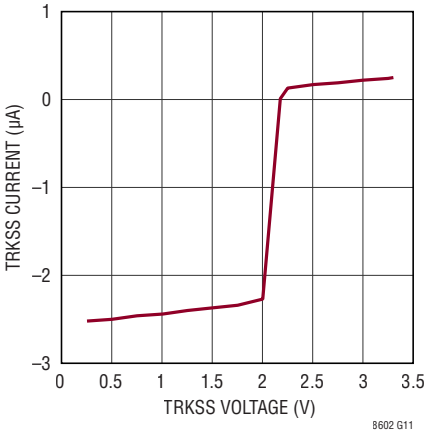
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V and PV_{IN3} = PV_{IN4} = 3.3V, unless otherwise noted.

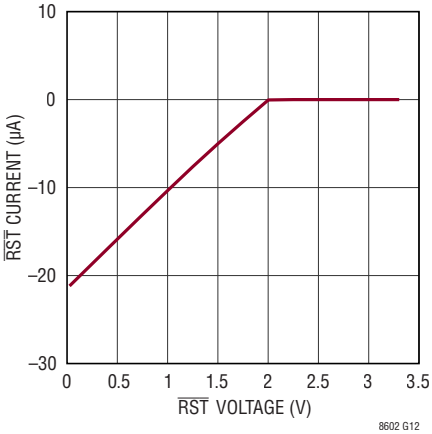
Switching Frequency vs Temperature



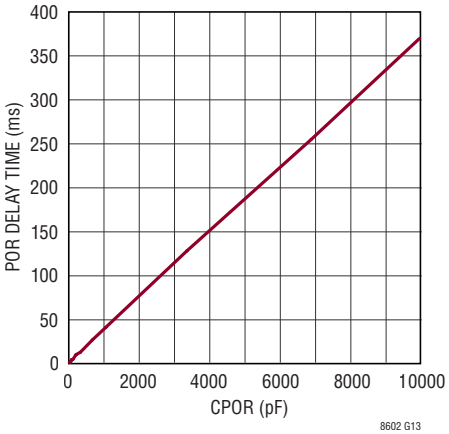
TRKSS Pull-Up Current vs Voltage



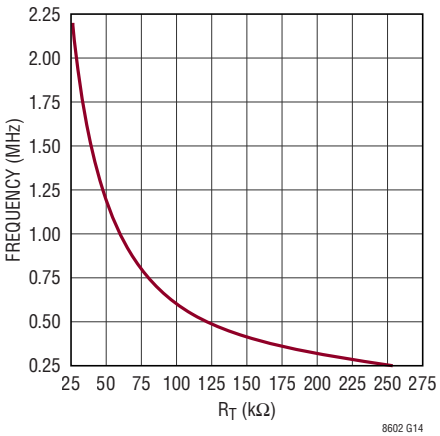
$\overline{RST}$ Pull-Up Current vs Voltage



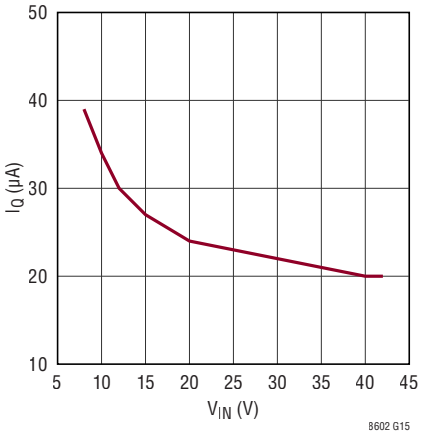
Power-On Reset Time vs CPOR



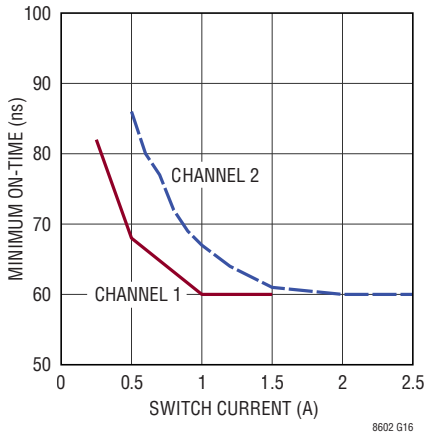
Switching Frequency vs R_T



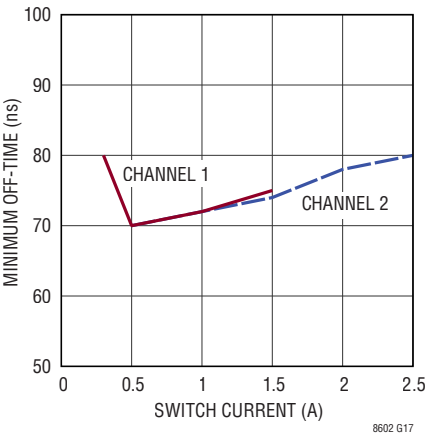
Quiescent Current vs V_{IN}



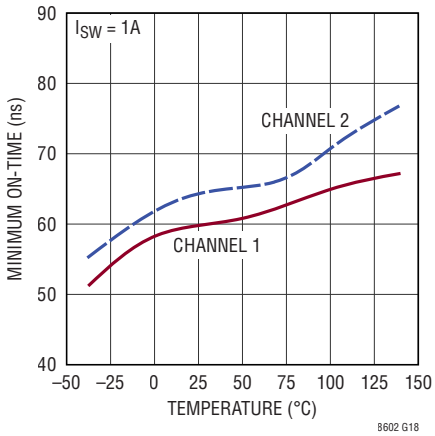
Minimum On-Time vs I_{SW}



Minimum Off-Time vs I_{SW}



Minimum On-Time vs Temperature

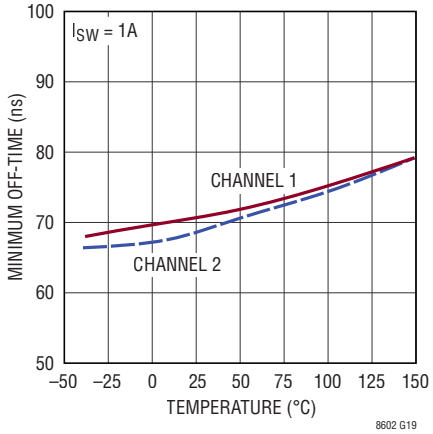


Rev. C

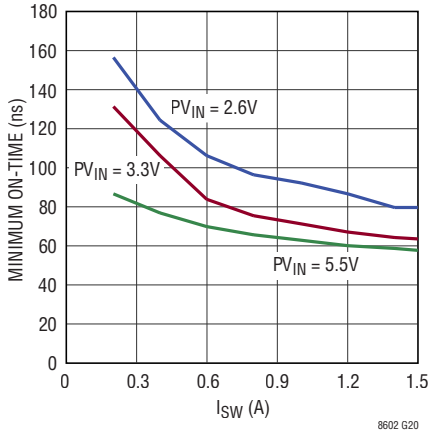
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V and PV_{IN3} = PV_{IN4} = 3.3V, unless otherwise noted.

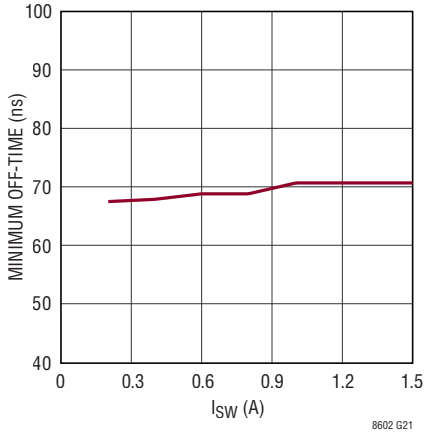
Minimum Off-Time vs Temperature



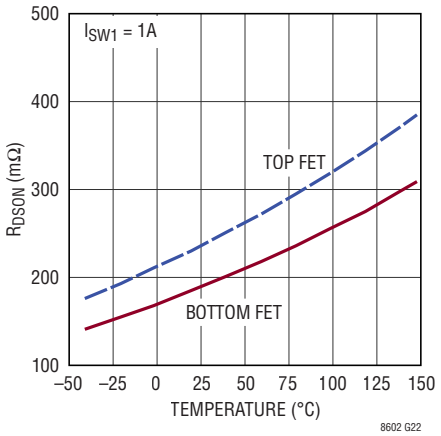
Channel 3/Channel 4 Minimum On-Time vs I_{SW}



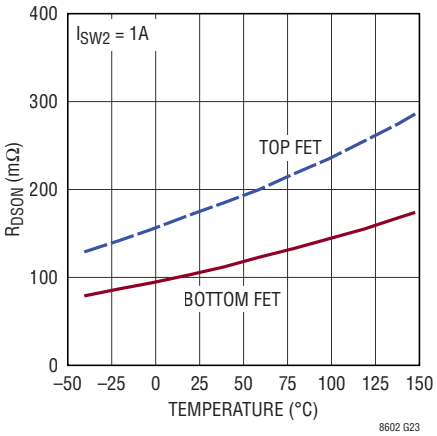
Channel 3/Channel 4 Minimum Off-Time vs I_{SW}



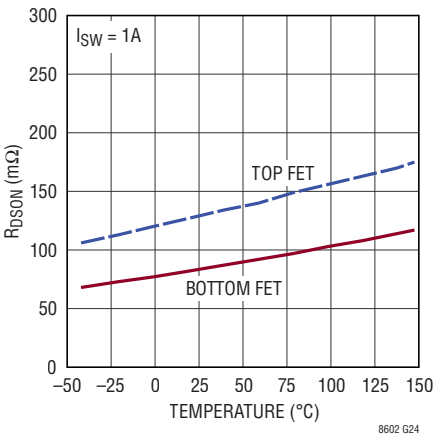
Channel 1 R_{DSON} vs Temperature



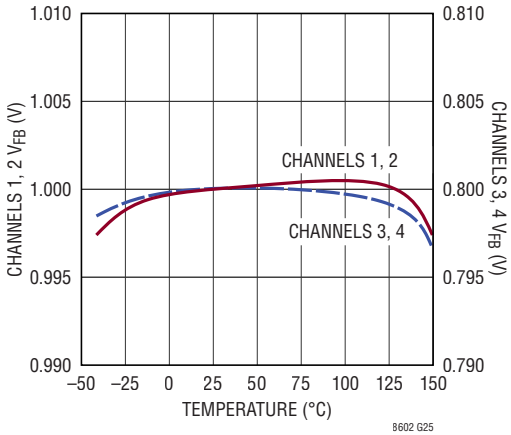
Channel 2 R_{DSON} vs Temperature



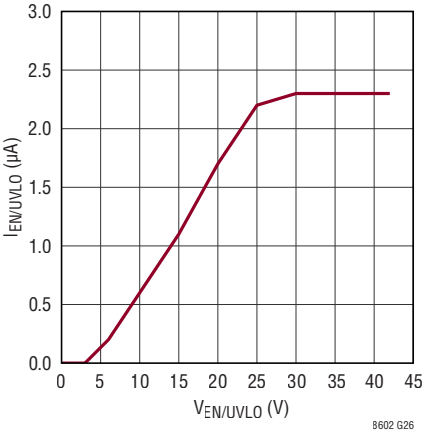
Channel 3/Channel 4 R_{DSON} vs Temperature



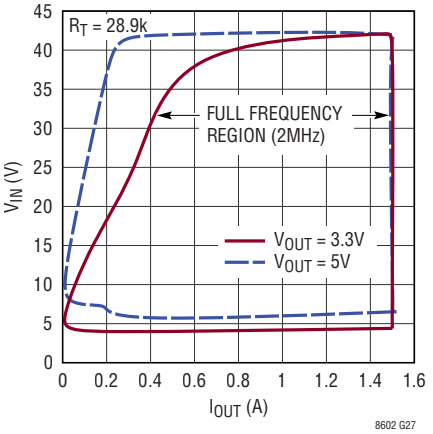
Feedback Voltage vs Temperature



EN/UVLO Current vs Voltage



Channel 1 Full Frequency V_{IN} vs Load Current

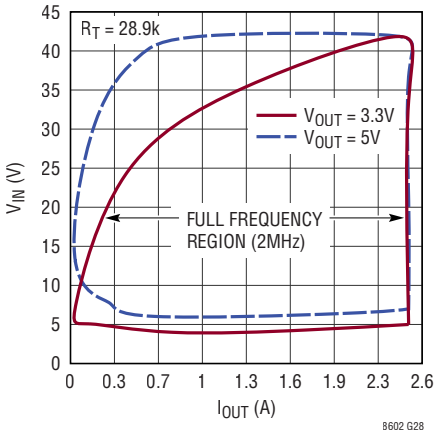


Rev. C

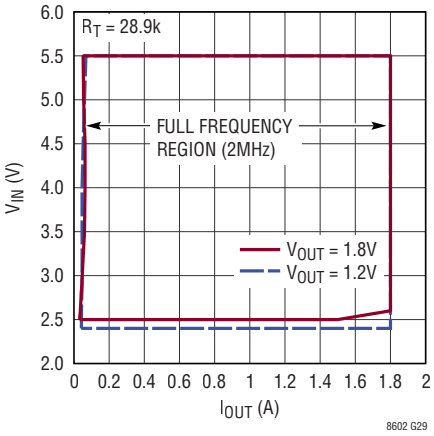
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = PV_{IN1} = PV_{IN2} = 12V, EN/UVLO = 3V and PV_{IN3} = PV_{IN4} = 3.3V, unless otherwise noted.

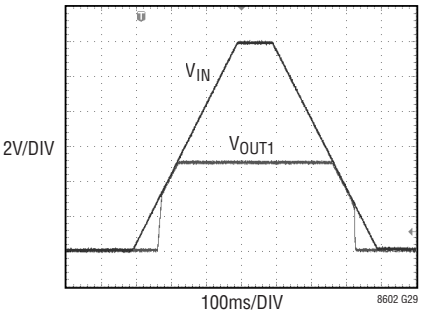
Channel 2 Full Frequency V_{IN} vs Load Current



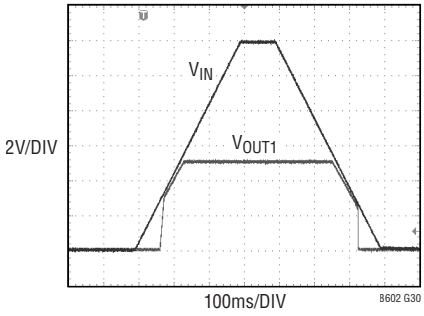
Channel 3, 4 Full Frequency V_{IN} vs Load Current



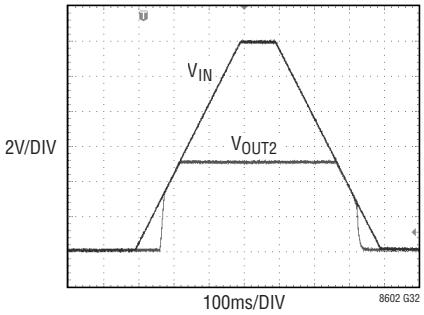
Channel 1 Start-Up and Dropout, R_L = 20Ω



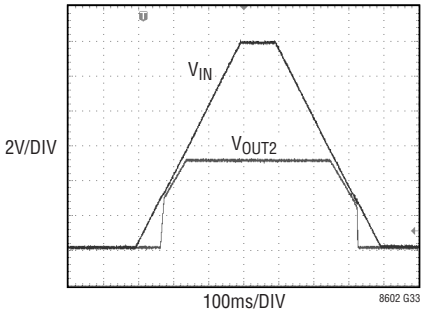
Channel 1 Start-Up and Dropout, R_L = 3.3Ω



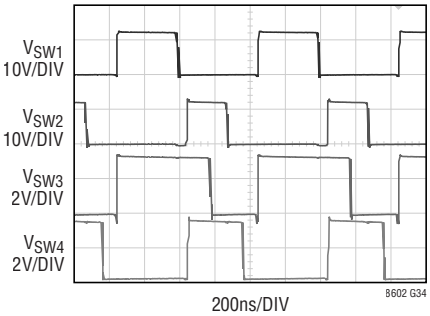
Channel 2 Start-Up and Dropout, R_L = 20Ω



Channel 2 Start-Up and Dropout, R_L = 2Ω

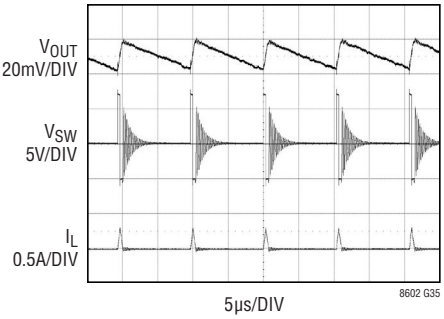


Full Frequency Waveforms



V_{OUT1} = 5V
V_{OUT2} = 3.3V
V_{OUT3} = 1.8V
V_{OUT4} = 1.2V

Light Load Waveforms

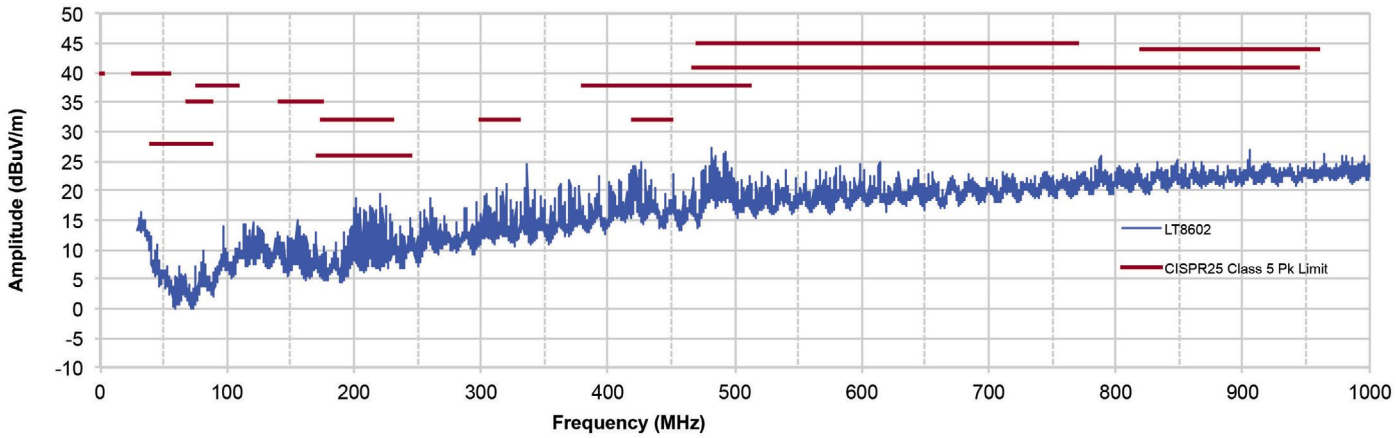


CHANNEL 1
$12V_{IN}$ TO $5V_{OUT}$ AT 10mA
V_{SYNC} = 0V

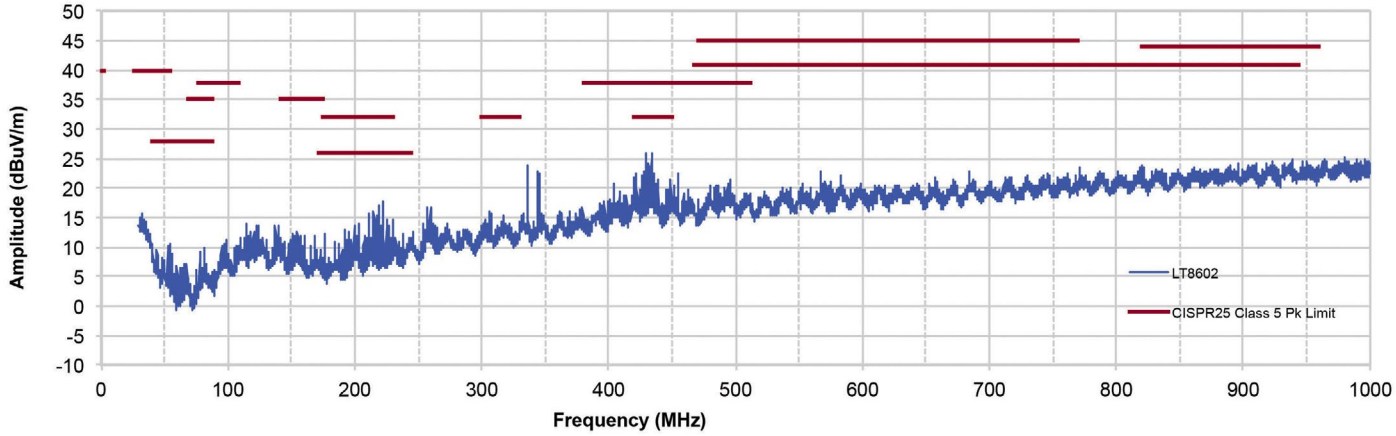
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C

Radiated EMI Performance, (CISPR25 Radiated Emission Tests with Class 5 Peak Limit)

Vertical Polarization



Horizontal Polarization



DC1949A Demo Board with EMI Filter Installed 14V_{IN}, 1A at All Outputs, F_{SW} = 2MHz

PIN FUNCTIONS (QFN/LXE)

BIAS (Pin 10/Pin 12): Power to the internal $INTV_{CC}$ regulator. Connect to an output ≥3.1V when such a supply is available. Leaving BIAS unconnected will result in a decrease in efficiency at light load. Decouple to ground with a low ESR capacitor.

BST1, BST2 (Pins 4, 5/Pins 6, 7): Boost Voltage for HV Channels. The Boost Voltage provides a drive voltage higher than PV_{IN} to the gate of the NMOS top switch.

CPOR (Pin 31/Pin 36): Power-On Reset Timer. Connect a capacitor from this pin to ground to program the power-on reset timer. CPOR has a 2µA pull-up current.

EN/UVLO (Pin 22/Pin 26): Enable/Undervoltage Lockout Input. The LT8602 is in low power shutdown when this pin is below 0.4V. Between 0.4V and 1.1V, the part will turn on the internal reference. A precision threshold at 1.2V (rising) enables the switching regulators. This allows the EN/UVLO pin to be used as an input undervoltage lockout by connecting to a resistor divider between V_{IN} and GND. When the EN/UVLO voltage is between 0.4V and 1.2V, the LT8602 input current will depend on the mode selected, the V_{IN} voltage and the EN/UVLO voltage. Connect to V_{IN} if the UVLO function is not needed.

FB1, FB2 (Pins 26, 25/Pins 31, 29): Feedback Input Pins for the High Voltage Converters. The converters regulate the corresponding feedback pin to the lesser of 1V or the voltage on the associated TRKSS pin.

FB3, FB4 (Pins 27, 24/Pins 32, 28): Feedback Input Pins for the Low Voltage Converters. The converters regulate the corresponding feedback pin to 800mV.

GND (Pins 2, 8, 9, 13, 16, 35, 38, 41/Pins 2, 3, 10, 11, 15, 18, 20, 22, 30, 39, 41, 43, 46): Ground. These pins must be soldered to PCB ground. The exposed pad (pin 41) must also be soldered to PCB ground.

$INTV_{CC}$ (Pin 28/Pin 33): Internal Regulator Bypass. Do not load the $INTV_{CC}$ pin with external circuitry. $INTV_{CC}$ is 3.1V when BIAS < 3.1V; 3.4V when BIAS > 3.4V; and equal to BIAS when BIAS is between 3.1V and 3.4V. Decouple to ground with a low ESR 4.7µF capacitor.

PG1, PG2 (Pins 1, 11/Pins 1, 13): Power Good Indicators for Channels 1 and 2. Open drain logic output pulls down until the corresponding FB pin rises above 0.92V but remains below 1.08V.

PG3, PG4 (Pins 40, 12/Pins 48, 14): Power Good Indicators for Channels 3 and 4. Open drain logic output pulls down until the corresponding FB pin rises above 0.736V but remains below 0.864V.

POREN (Pin 39/Pin 47): Power On Reset Enable. This is a logic input that starts the ramp on the POR timing capacitor. This input has a weak pull-up.

PV_{IN1}, PV_{IN2} (Pins 37, 14/Pins 44, 45, 16, 17): Input Supply Voltage to HV Channels 1 and 2, respectively. These pins are independent and can be powered from different sources if necessary. Bypass each input with a low ESR capacitor to the adjacent GND pin.

PV_{IN3}, PV_{IN4} (Pins 34, 17/Pins 40, 21): Input Supply Voltage to low voltage Channels 3 and 4. These pins are typically connected to one of the high voltage converter outputs and should be locally bypassed with a low ESR capacitor. PV_{IN3} and PV_{IN4} are independent and do not need to be connected to the same supply voltage.

$\overline{RST}$ (Pin 32/Pin 37): Power-On Reset Output. CMOS output with weak pull-up, this pin is held low until the POR times out.

RT (Pin 29/Pin 34): Frequency Programming Resistor. Connect a resistor from this pin to ground to set the internal oscillator frequency.

PIN FUNCTIONS (QFN/LXE)

RUN3, RUN4 (Pins 30, 18/Pin 35, 23): Run Inputs for the low voltage converters.

SW1 (Pin 3/Pins 4, 5): Channel 1 Switch Node. This is the output of the internal power switches for Channel 1.

SW2 (Pins 6, 7/Pins 8, 9): Channel 2 Switch Node. This is the output of the internal power switches for Channel 2. These pins must be connected together.

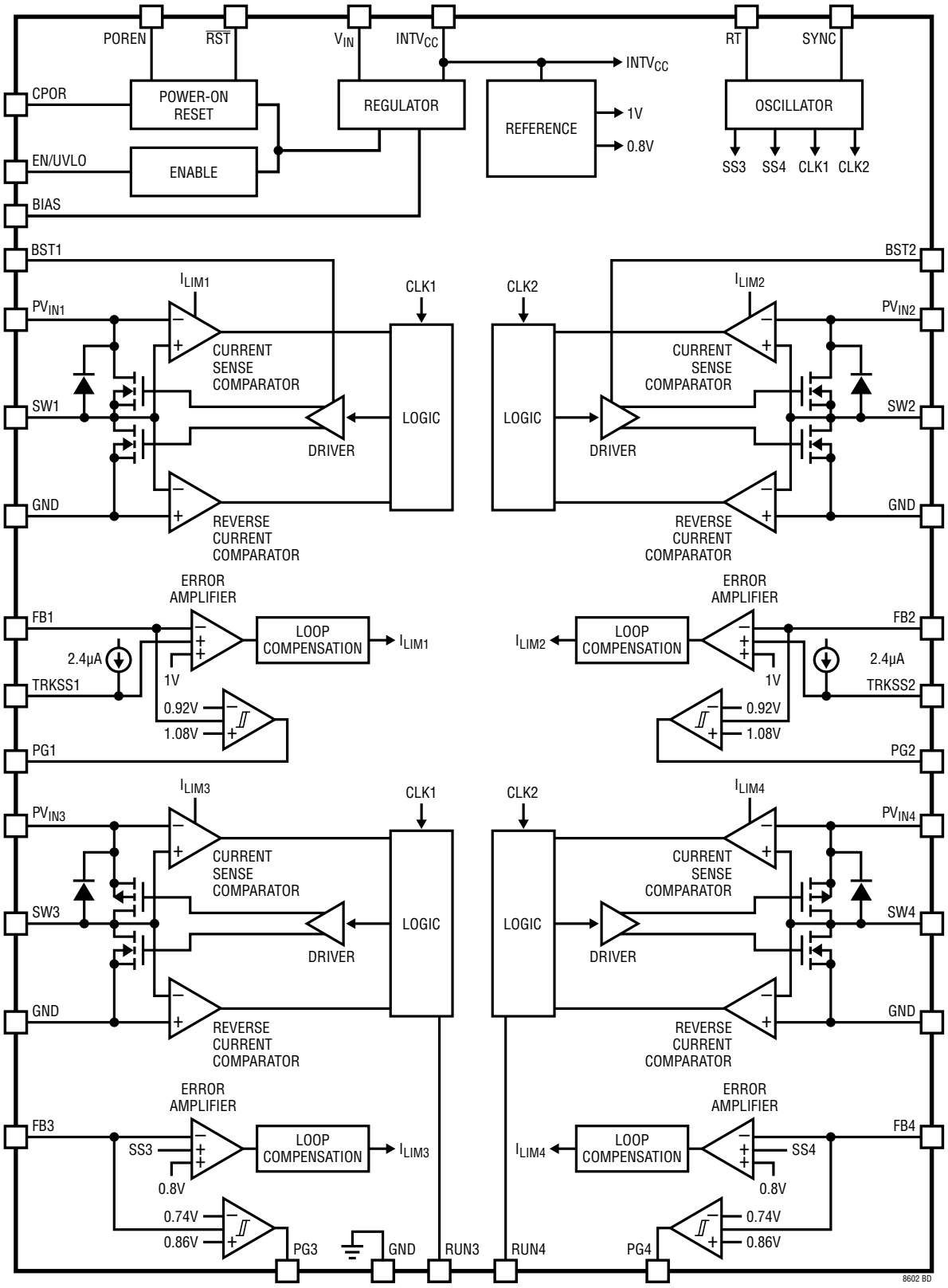
SW3, SW4 (Pins 36, 15/Pins 42, 19): Switch Nodes for low voltage converters. These are the outputs of the internal power switches for Channels 3 and 4.

SYNC (Pin 33/Pin 38): Clock Synchronization Input. A digital input to allow the LT8602 to synchronize its switching frequency to an external clock. If clock synchronization is not used, connect this pin to ground to enable low ripple burst mode or connect high to enable pulse skip operation of the synchronous converters. Do not allow SYNC to float.

TRKSS1, TRKSS2 (Pins 21, 20/Pins 25, 24): Track/Soft-Start Inputs for the High Voltage Converters. When this pin is below 1V, the converter regulates the FB pin to the TRKSS voltage instead of the internal reference. The TRKSS pin has a 2.4µA pull-up current. TRKSS may be left floating

V_{IN} (Pin 23/Pin 27): Input Supply Voltage to Internal Functions. This pin is independent from any PV_{IN} pin and can be powered from different sources if necessary. V_{IN} must be above 3V for the part to operate.

BLOCK DIAGRAM



OPERATION

The LT8602 is a quad channel, constant frequency, current mode, monolithic buck switching regulator with power-on reset. All channels are synchronized to a single oscillator. Two of the channels are high voltage (up to 42V input) while the other two are low voltage (up to 5.5V input) and are typically powered from the high voltage buck outputs.

Start-Up

When enabled by setting the EN/UVLO voltage above its threshold, the LT8602 starts charging the $INTV_{CC}$ capacitor from V_{IN}. If BIAS is higher than 3.1V, BIAS supplies current to the $INTV_{CC}$ regulator to reduce V_{IN} quiescent current.

High Voltage Buck Regulators

Each high voltage channel is a synchronous buck regulator that operates from an independent PV_{IN} pin. The internal top power MOSFET is turned on at the beginning of each oscillator cycle, and turned off when the current flowing through the top MOSFET reaches a level determined by the error amplifier. The error amplifier measures the output voltage through an external resistor divider tied to the FB pin to control the peak current in the top switch. The reference of the error amplifier is determined by the lower of the internal 1V reference and the voltage at its TRKSS pin.

While the top MOSFET is off, the bottom MOSFET is turned on for the remainder of the oscillator cycle or until the inductor current starts to reverse. If overload conditions result in more than 2A (Ch 1) or 3.3A (Ch 2) flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

Low Voltage Buck Regulators

Each low voltage channel is a synchronous buck regulator that operates from an independent PV_{IN} pin. The PV_{IN} pins have an undervoltage lockout set at 2.35V. Each internal top power MOSFET is turned on at the beginning of each oscillator cycle, and turned off when the current flowing through the top MOSFET reaches a level determined by the error amplifier. The error amplifier measures the output voltage through an external resistor divider tied to the FB pin to control the peak current in the top switch. The reference of the error amplifier is an internal 800mV reference. Each LV channel has a RUN pin to allow power sequencing and an internal soft-start circuit ramps the output voltage up in 1ms.

While the top MOSFET is off, the bottom MOSFET is turned on for the remainder of the oscillator cycle or until the inductor current starts to reverse. If overload conditions result in more than 2.4A flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

Multiphase Switching

The oscillator generates two clock signals 180° out of phase. Channels 1 and 3 operate on CLK1, while channels 2 and 4 operate on CLK2. Since a buck regulator only draws input current during the top switch on cycle, multiphase operation reduces peak input current and doubles the input current frequency. These effects reduce input current ripple and reduce the input capacitance required.

Light Load Operation

At light load, the regulators operate in low ripple burst mode. Low ripple burst mode shuts down most internal circuitry between switch on cycles to conserve power while still retaining low ripple at the output.

Undervoltage Lockout

The EN/UVLO pin is used to put the LT8602 in shutdown, reducing the input current to less than 1µA. The accurate 1.2V threshold of the EN/UVLO pin allows a programmable V_{IN} undervoltage lockout through an external resistor divider tied to the EN/UVLO pin. A 50mV (typ) hysteresis voltage on the EN/UVLO pin prevents switching noise from inadvertently shutting down the LT8602.

OPERATION

Power Good Comparators

Each channel has a power good comparator that trips when the feedback pin is above or below its reference voltage by more than 8%. The PG output pins are open drain. The PG pin for each channel is pulled low when the corresponding output is out of regulation. The PG outputs are not valid until $INTV_{CC}$ rises to 2.7V

Power-On Reset Timer

The LT8602 includes a power-on reset timer. The power-on reset time is adjustable using an external capacitor on the CPOR pin. The timer is enabled by the POREN pin.

The $\overline{RST}$ pin is the output of the POR timer and is an open-drain output with a weak internal pull-up. The $\overline{RST}$ pin is valid when the LT8602 is enabled and $INTV_{CC}$ is above 2.7V.

APPLICATIONS INFORMATION

Setting the Output Voltages

The output voltages are set by the resistor dividers on the outputs as shown in Figure 1. The formula used is:

$$R1 = R2 \bullet \left(\frac{V_{OUTx}}{FB_{REF}} - 1 \right)$$

where V_{OUTx} is the output voltage of regulator x and FB_{REF} is the feedback reference voltage. FB_{REF} is 1V for the high voltage regulators (1 and 2) and 800mV for the low voltage channels (3 and 4). Use 1% resistors in the dividers. R2 should be 200k or less to avoid noise problems.

To improve the frequency response, a feedforward capacitor C_{ff} may be used. Typical values are 10pf to 100pf. Great care should be taken to route the V_{FB} node away from noise sources, such as the inductor or a SW line.

Switching Frequency

The LT8602 uses a constant frequency architecture that can be programmed from 250kHz to 2.2MHz by tying a resistor from the RT pin to ground. Table 1 shows the value of R_T for common switching frequencies.

Table 1. Switching Frequency vs R_T Value

SWITCHING FREQUENCY (MHz)	R_T (kΩ)
0.25	254
0.35	179
0.5	124
0.75	81.2
1.0	60.4
1.25	47.6
1.5	39.4
1.75	33.3
2.0	28.9
2.2	26.3

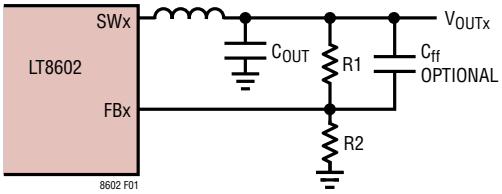


Figure 1. Feedback Resistor Divider

The following equation approximates the values shown in Table 1:

$$R_T = \frac{61.9}{f_S - 0.009} - 1.9$$

where R_T is in kΩ and f_S is in MHz.

Selection of the operating frequency is mainly a trade-off between efficiency and component size. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The advantage of low frequency operation is higher efficiency.

The high switching frequency also decreases the duty cycle range because of finite minimum on- and off-times which are independent of the switching frequency. The top switch in the high voltage channel has a minimum on-time of 60ns and minimum off-time of of 70ns. The top switch in the low voltage channel has a minimum on-time of 70ns and minimum off-time of 70ns. The minimum and maximum duty cycles are:

$$DC_{MIN} = f_S \bullet t_{ON(MIN)}$$

$$DC_{MAX} = 1 - f_S \bullet t_{OFF(MIN)}$$

where f_S is the switching frequency, $t_{ON(MIN)}$ is the minimum switch on-time, and $t_{OFF(MIN)}$ is the minimum switch off-time. These equations illustrate how duty cycle range increases when the switching frequency decreases.

The internal oscillator of the LT8602 can be synchronized to an external 250kHz to 2.2MHz clock signal on the SYNC pin.

APPLICATIONS INFORMATION

V_{IN} Voltage Range

The LT8602's minimum operating voltage is 3V. To program a higher minimum operating voltage, use a resistor divider between the V_{IN} pin and the EN/UVLO pin. The EN/UVLO threshold is 1.2V. The EN/UVLO pin has 50mV of hysteresis to prevent glitches from falsely disabling the LT8602.

The UVLO circuit is shown in Figure 3, Reverse Protection Diodes. The calculation for the lockout voltage is:

$$V_{IN(UVLO)} = \frac{R_{UV1}+R_{UV2}}{R_{UV2}} \bullet 1.2V$$

PV_{IN} Voltage Range

Each switching regulator channel operates from its own PV_{IN} pin (PV_{IN1} to PV_{IN4}). The PV_{IN} pin can be connected to either an independent voltage supply or a high voltage channel output. The PV_{IN1} and PV_{IN2} voltage range is 3.0V to 42V. The PV_{IN3} and PV_{IN4} voltage range is 2.6V to 5.5V.

The minimum PV_{IN} voltage to regulate output voltage at full frequency is:

$$PV_{INx(MIN)} = \frac{V_{OUTx}}{DC_{MAX}}$$

Where DC_{MAX} is the maximum duty cycle (refer to Switching Frequency section) for that channel. If PV_{IN} is below the calculated minimum voltage, the channel starts to skip switch off cycles. At low input voltages the part will turn on the top switch for longer than a full switch cycle in order to extend the effective duty cycle. When the part is extending the effective duty cycle the switching frequency will drop to one half (or less) of the programmed frequency.

The maximum PV_{IN} voltage to regulate output voltage at full frequency is:

$$PV_{INx(MAX)} = \frac{V_{OUTx}}{DC_{MIN}}$$

Where DC_{MIN} is the minimum duty cycle (refer to Switching Frequency section) for that channel. If PV_{IN} is above the calculated maximum voltage, the channel starts to skip switch on cycles (pulse-skipping). In this case, the channel switching frequency will no longer be the programmed frequency. The output will continue to regulate, but the peak inductor current and output ripple will increase significantly.

Inductor Selection

Inductor selection involves inductance, saturation current, series resistance (DCR) and magnetic loss.

A good starting point for the inductance values are:

$$Lx = Kx \bullet \frac{V_{OUTx}}{PV_{INx}} \bullet \frac{PV_{INx} - V_{OUTx}}{f_S}$$

where f_S is the switching frequency in MHz, Lx is in µH, V_{OUTx} is the channel output voltage and K1 = 1.6, K2 = 1.0 and K3 and K4 = 1.3.

Once the inductance is selected, the inductor current ripple and peak current can be calculated:

$$\Delta I_{Lx} = \frac{V_{OUTx}}{Lx \bullet f_S} \bullet \left(1 - \frac{V_{OUTx}}{PV_{INx(MAX)}}\right)$$

$$I_{Lx(PEAK)} = I_{OUTx(MAX)} + \frac{\Delta I_{Lx}}{2}$$

To guarantee sufficient output current, peak inductor current must be lower than the switch current limit (I_{LIM}).

To keep the efficiency high, the inductor series resistance (DCR) should be as small as possible (must be <0.1Ω for channels 1, 3 and 4; <0.06Ω for channel 2), and the core material should be intended for the chosen switching frequency. Table 2 lists several vendors and suitable inductor series.

Table 2. Inductor Vendors

VENDOR	SERIES	WEBSITE
TDK	SLF, VLC, VLF	www.tdk.com
Sumida	CDRH, CDR, CDMC	www.sumida.com
Coilcraft	XAL, XFL, MSS	www.coilcraft.com
NIC	NPIM, NPIS	www.niccomp.com
Würth	TPC, SPC, PD, PDF, PD3	www.we-online.com

APPLICATIONS INFORMATION

Of course, such a simple design guide will not always result in the optimum inductors for the applications. A larger value inductor provides a slightly higher maximum load current and will reduce the output voltage ripple. A larger value inductor can result in higher efficiency if the DCR and magnetic losses are the same. However, for inductors of the same dimensions, the larger value inductor has higher DCR. The trade-off between inductance and DCR is not always obvious. Use experiments to find optimum inductors.

Low inductance may result in discontinuous mode operation, which is acceptable, but reduces maximum load current. For details of maximum output current and discontinuous mode operation, see the Linear Technology Application Note 44. For duty cycles greater than 50%, there is a minimum inductance required to avoid subharmonic oscillations.

$$L_{MINx} = \frac{1.05 \bullet (V_{OUTx} + V_{BOTx})}{f_S}, \text{ chs 1, 3 and 4}$$

$$L_{MINx} = \frac{0.70 \bullet (V_{OUTx} + V_{BOTx})}{f_S}, \text{ ch 2}$$

where V_{OUTx} is the output voltage; V_{BOTx} is the voltage across the bottom switch; f_S is the switching frequency in MHz and L_{MINx} is in µH. If the frequency is synchronized over a range, use the lowest frequency to determine L_{MINx}.

Shorted Output Protection

The LT8602 will tolerate a shorted output. If the bottom MOSFET current exceeds the valley current limit at the start of a clock cycle, the top MOSFET is kept off until the overcurrent situation clears. This prevents the buildup of inductor current during a shorted output.

Input Capacitor Selection

Bypass each PV_{IN} pin of the LT8602 with a ceramic capacitor of X5R (max 85°C), X7R (max 125°C), or X8R (max 150°C) type as appropriate.

Step-down converters draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT8602 input and to force this switching current into a tight local loop, minimizing EMI. The input capacitor must have low impedance at the switching frequency to do this effectively and it must have an adequate ripple current rating.

The worst case ripple current is when V_{OUT} is one half of PV_{IN}. In this case, the ripple current is:

$$I_{CIN(RMS)} = \frac{I_{OUT}}{2}$$

A reasonable value for the input capacitor is:

$$C_{IN} = \frac{4.7\mu F \text{ (for Chs 1, 3, 4) or } 10\mu F \text{ (for Ch 2)}}{f_S}$$

where f_S is the switching frequency in MHz.

Careful placement of C_{IN} is essential to get the lowest ripple and EMI. C_{IN} should be placed as close to the PV_{IN} pin as possible and on the same side of the PC board. The layer immediately below the component traces should be an unbroken ground plane. The ground side of C_{IN} should have at least 2 vias to the ground plane as close to C_{IN} as possible. This provides a high frequency return path directly under the PV_{IN} to C_{IN} trace. This minimizes loop area of the high frequency, high current path from PV_{IN} to C_{IN} and back to the GND exposed pad. See Figure 8, Recommended PCB Layout.

A word of caution is in order regarding the use of ceramic capacitors at the input. A ceramic input capacitor can combine with stray inductance to form a resonant tank circuit back to the supply. If power is applied quickly (for example by plugging the circuit into a live power source), this tank can ring, as much as doubling the input voltage. The solution is to either clamp the input voltage or dampen the tank circuit by adding a lossy capacitor in parallel with the ceramic capacitor. For details, see Linear Technology Application Note 88.

APPLICATIONS INFORMATION

Output Capacitor Selection

The output capacitor performs two functions. First, it filters the inductor current to generate an output with low voltage ripple. Second, it stores energy to minimize overshoot during transient loads. Because the LT8602 operates at a high frequency, minimal output capacitance is necessary. The control loop operates well with or without the presence of output capacitor series resistance (ESR). Ceramic capacitors, which achieve very low output ripple and small circuit size, are therefore an option.

You can estimate output ripple with the following equations:

$$V_{RIPPLE} = \frac{\Delta I_L}{8 \bullet f_S \bullet C_{OUT}}, \text{ for ceramic}$$

$$V_{RIPPLE} = \Delta I_L \bullet ESR, \text{ for aluminum or tantalum.}$$

where V_{RIPPLE} is the peak-to-peak output ripple, f_S is the switching frequency in MHz, ΔI_L is the peak-to-peak ripple current in the inductor, C_{OUT} is the output capacitor value in µF and ESR is the output capacitor series resistance.

Another constraint on the output capacitor is that it must have greater energy storage than the inductor. When the load current steps from high to low, the stored energy in the inductor transfers to the output and the resulting voltage step should be small compared to the regulation voltage. For a 5% overshoot, this requirement indicates:

$$C_{OUT} \geq 10 \bullet L \bullet \left(\frac{I_{LIM}}{V_{OUT}} \right)^2$$

where I_{LIM} is the maximum switch current limit.

The low ESR and small size of ceramic capacitors make them the preferred type for LT8602 applications. Not all ceramic capacitors are the same, however. Many of the higher value capacitors use poor dielectrics with high temperature and voltage coefficients. In particular, Y5V and Z5U types lose a large fraction of their capacitance with applied voltage and at temperature extremes. Because loop stability and transient response depend on the value of C_{OUT}, this loss may be unacceptable. It is best to use X5R (max 85°C), X7R (max 125°C), or X8R (max 150°C) types as appropriate considering operating temperature.

Electrolytic capacitors are also an option. The ESRs of most aluminum electrolytic capacitors are too large to deliver low output ripple. Tantalum, as well as newer, lower-ESR, organic electrolytic capacitors intended for power supply use are suitable. Chose a capacitor with a low enough ESR for the required output ripple. Because the volume of the capacitor determines its ESR, both the size and the value will be larger than a ceramic capacitor that would give similar ripple performance. One benefit is that the larger capacitance may give better transient response for large changes in load current. Table 3 lists several capacitor vendors.

Table 3. Low ESR Capacitor Vendors

VENDOR	SERIES	TYPE
Taiyo-Yuden www.t-yuden.com		Ceramic
TDK www.tdk.com		Ceramic
Kemet www.kemet.com	 T494, T495 T510, T520, T525, T530 A700	Ceramic Tantalum Tantalum Organic Polymer Alum. Organic Polymer
Panasonic www.panasonic.com	 SP-CAP	Ceramic Alum. Organic Polymer
AVX www.avx.com	 TPS, TES, TCH	Ceramic Tantalum

BST and SW Pin Considerations

The high voltage channels require a voltage above PV_{IN} to drive the gates of the top NFET switches. Connect an external capacitor between the BST and SW pins. An internal MOS switch connects BST to the internal $INTV_{CC}$ supply during the switch off cycles. Then BST is boosted above SW during the switch on cycles. In most cases, a 0.1µF capacitor will work well.

Soft-Start

The LT8602 has a soft-start pin for each high voltage channel and internal soft-start for each low voltage channel. The low voltage channel soft-start is set to 1ms.

On the high voltage channels, the feedback pin voltage is regulated to the lower of the corresponding TRKSS

APPLICATIONS INFORMATION

pin and the internal reference of 1V. A capacitor from the TRKSS pin to ground is charged by an internal 2.4µA current source resulting in an output ramping linearly from 0V to the regulated voltage. The duration of the ramp is:

$$t_{SS} = C_{TRKSS} \bullet \frac{1V}{2.4\mu A}$$

where t_{SS} is the ramping time in seconds and C_{TRKSS} is the capacitance on the TRKSS pin in F.

The TRKSS pin is pulled down at start-up until $INTV_{CC}$ has reached operating voltage. It is also pulled down in an undervoltage condition, either the internal lockout on PV_{IN} or the programmable EN/UVLO pin. The resistance when TRKSS is pulled down is 400Ω. Pulling TRKSS to ground does not guarantee the channel will stop switching.

The TRKSS pin can also be used to allow the output to track another regulator, either the other HV channel or an external regulator. Use a resistor divider from the controlling output to the TRKSS pin. Figure 2 shows the circuit for channel 2 tracking V_{OUT1} as well as output waveforms for coincident and ratiometric tracking.

R2 should be 10k or less to minimize the offset from the 2.4µA pull-up current.

Another easy method to ratiometrically track channels 1 and 2 is to tie both TRKSS1 and TRKSS2 together with a single capacitor to ground. This will double the soft-start current.

For applications with a start-up sequence that requires a PG pin be tied to a TRKSS input, a 10k or less resistor must be used as an external pull-up. The soft-start time with this configuration can be approximated by:

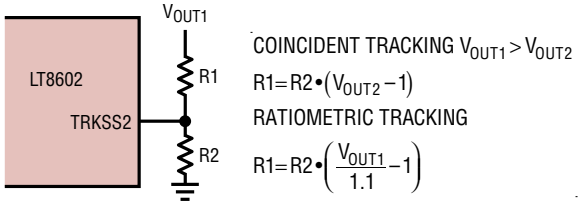
$$t_{SS} = 0.5 \bullet R_{PULLUP} \bullet C_{TRKSS}$$

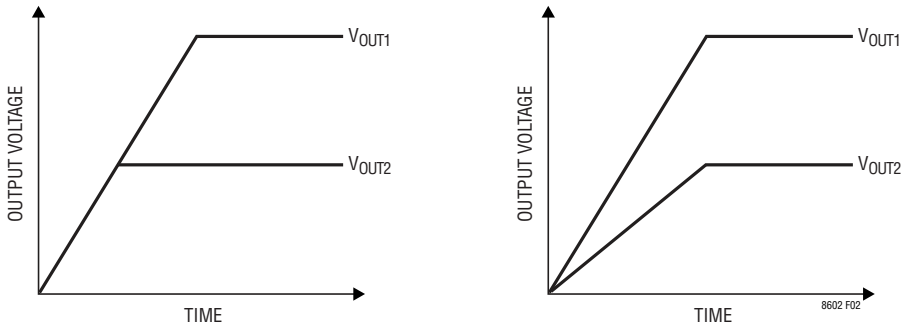
A more exact formula, that includes the dependence on the pull-up voltage, V_{PULLUP}, is given by:

$$t_{SS} = -R_{PULLUP} \bullet C_{TRKSS} \bullet \log_e\left(1 - \frac{1V}{V_{PULLUP}}\right)$$

Reverse Protection

In battery charging applications or in battery backup systems, an output will be held high by the battery when the input to the LT8602 is absent. If the V_{IN} and PV_{IN} pins are floated and the LT8602 is enabled, the internal circuitry will pull its quiescent current through the SW pin of the output that is held high. This is acceptable if





(2a) Coincident Tracking **(2b) Ratiometric Tracking**

Figure 2. Tracking Circuit

APPLICATIONS INFORMATION

the system can tolerate a small current (<100µA) in this state. If the LT8602 is disabled, the SW pin current will drop to essentially zero. However, if the V_{IN} or PV_{IN} pin is grounded while the output is held high, an external diode is required at the V_{IN}/PV_{IN} pin to prevent current being pulled out of the V_{IN}/PV_{IN} pin. An example is shown in Figure 3. In this case, both OUT1 and OUT3 are held high by batteries. PV_{IN1} must be diode protected, as well as PV_{IN3} if it is connected to an external supply.

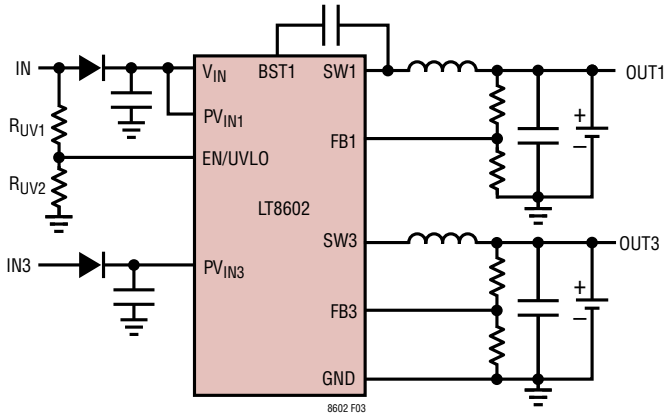


Figure 3. Reverse Protection Diodes

Burst Mode Operation

To improve efficiency at light loads, the LT8602 automatically switches to Burst Mode operation which minimizes the switching loss and keeps the output voltage ripple small. In Burst Mode operation, most of the circuits are shut down between switch-on bursts to minimize power loss. If at least one channel remains full frequency, the oscillator remains on and all bursts are synchronized to the appropriate phase of the oscillator (Figure 4). If all four channels go into Burst Mode operation, the oscillator will also shut off between bursts with a further savings in power (Figure 5). Because the channels of the LT8602 may have different loads, channels can have different switching frequencies when in Burst Mode operation.

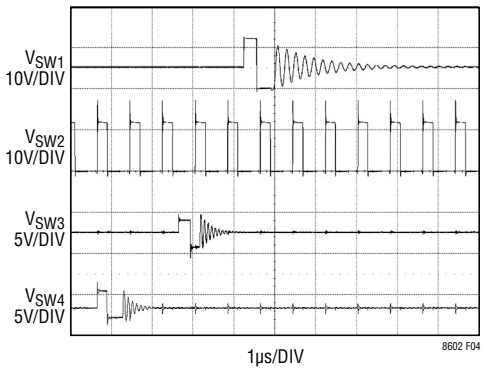


Figure 4. Burst Mode SW Waveforms with Oscillator Running

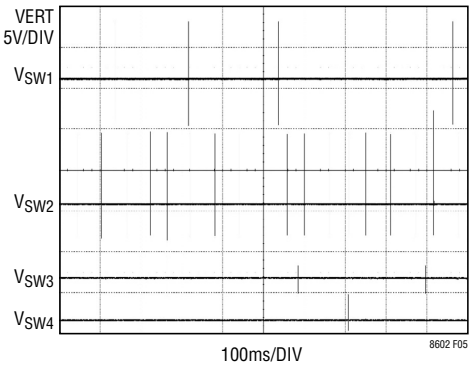


Figure 5. Burst Mode SW Waveforms with All Channels in Burst Mode

Mode Selection and Synchronization

To select low ripple Burst Mode operation, tie the SYNC pin below 0.3V (this can be ground or a logic low output). To select pulse-skipping operation, tie the SYNC pin above 1.2V. To synchronize the LT8602 oscillator to an external frequency connect a square wave (with 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below SYNC V_{IL} and peaks above SYNC V_{IH} (up to 6V).

The LT8602 will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will pulse skip to maintain regulation. The LT8602 may be synchronized over a 250kHz to 2.2MHz range. The R_T resistor should be chosen to set the LT8602 switching frequency equal to the synchronization input. If a range of frequencies is used, set R_T to the center of the range. For example, if the synchronization signal will be 400kHz to 600kHz, the R_T should be selected for 500kHz. The SYNC lock range is ±20% of the R_T set frequency.

For some applications it is desirable for the LT8602 to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. First is that the clock stays awake at all times and all switching cycles are aligned to the clock. Second is that full switching frequency is

APPLICATIONS INFORMATION

reached at lower output load than in Burst Mode operation. These two differences come at the expense of increased quiescent current. To enable pulse-skipping mode, the SYNC pin is tied high either to a logic output or to the $INTV_{CC}$ pin.

Do not leave the SYNC pin floating.

Power Good Comparators

Each channel of the LT8602 has a power-good comparator that monitors the corresponding feedback voltages when the LT8602 is enabled. The threshold of power-good comparator is 0.92V to 1.08V for the high voltage channels, and 736mV to 864mV for the low voltage channels. The PG outputs are open-drain and require an external pull-up resistance value of 20k or less.

Power-On Reset Timer

The power-on reset timer circuit provides a programmable reset timer. The POREN pin is the enable for the reset timer. The $\overline{RST}$ output is an open-drain output with a weak internal pull-up (100k to ~2V). The weak pull-ups eliminate the need for external pull-ups when the rise time of these pins is not critical. The open-drain configuration allows wired-OR connections of the $\overline{RST}$ pin.

The power-on reset timeout period, $t_{\overline{RST}}$, can be programmed by connecting a capacitor, C_{POR}, between the CPOR pin and ground. The value of $t_{\overline{RST}}$ is calculated by:

$$t_{\overline{RST}} = 35.2 \bullet C_{POR}$$

Where C_{POR} is in pF and $t_{\overline{RST}}$ is in microseconds. When POREN is enabled, the CPOR pin is ramped up at 2µA until it reaches 1.2V. The current reverses and ramps down at 20µA. When it reaches 0.2V, it ramps back up at 2µA. This cycle repeats a total of 64 times, then the $\overline{RST}$ pin is set high. For example, using a capacitor value of 8.2nF gives a 289ms reset timeout period. The accuracy of $t_{\overline{RST}}$ will be limited by the accuracy and temperature coefficient of the capacitor C_{POR}. Extra parasitic capacitance on the CPOR pin, such as probe capacitance, can affect $t_{\overline{RST}}$. Figure 6 shows the power on reset timing. CPOR values above 10nF are not recommended.

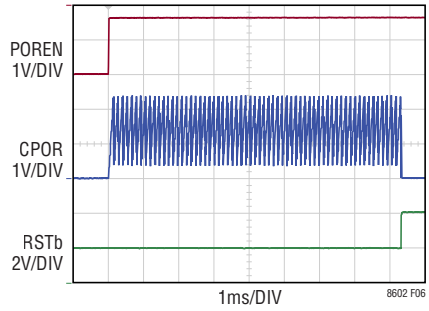


Figure 6. Power-On Reset Timing C_{POR} = 230pF

Sequencing

The LT8602 provides great flexibility in sequencing the 4 channels and the power-on reset timer. Each channel has a power good output (PG1 to PG4) and a controlling input (TRKSS1 and 2, RUN3 and 4). The POR has a control input (POREN) and a reset output ($\overline{RST}$). All 5 outputs are open-drain. All 5 inputs are active high and 3 of them (TRKSS1 and 2, POREN) have internal pull-up currents to reduce external component counts. The soft-start function on the TRKSS pins will work when using sequencing; simply connect the capacitor to the TRKSS pin, connect an external pull-up resistor of value 10k or less and use the desired PG output to short the cap. A sequencing example is shown in Figure 7.

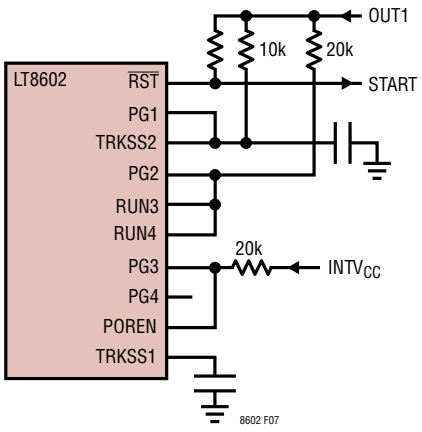


Figure 7. Sequencing the Outputs and POR

APPLICATIONS INFORMATION

In this example, channel 1 starts first, and soft-starts according to the cap on TRKSS1. Once OUT1 has reached regulation, channel 2 soft-starts. When OUT2 is good, channels 3 and 4 start up. When OUT3 is in regulation, then the POR is started. One caution when connecting RUN pins to TRKSS pins: the TRKSS channel will start ramping immediately, but the RUN channel will not start until the voltage reaches the RUN threshold.

The EN/UVLO pin has two thresholds enabling three modes (see Figure 8: EN/UVLO Thresholds). When EN/UVLO is below the shutdown threshold, the 8602 is in low power shutdown and draws less than 1µa from V_{IN} under all conditions. The shutdown threshold is between 0.4V and 1.1V. Once EN/UVLO has risen above the shutdown threshold but is still below the undervoltage threshold, the internal bias circuits start up but the switching regulators are kept off. The input current in this region can be as high as 400µa, depending on the mode selected, V_{IN} and direction of EN/UVLO. Since the internal reference is now on, it establishes an accurate undervoltage threshold of 1.2V (typ). When EN/UVLO rises above the undervoltage threshold, then the switching regulators are turned on and normal operation begins. This allows a programmable undervoltage lockout by connecting a resistor divider from EN/UVLO to V_{IN}.

If the EN/UVLO function is not needed, the pin can be connected directly to V_{IN}. If only enable is needed and the undervoltage lockout is not needed, the EN/UVLO pin can be connected directly to a logic output with a V_{OH} of at least 1.25V and a V_{OL} less than 0.4V.

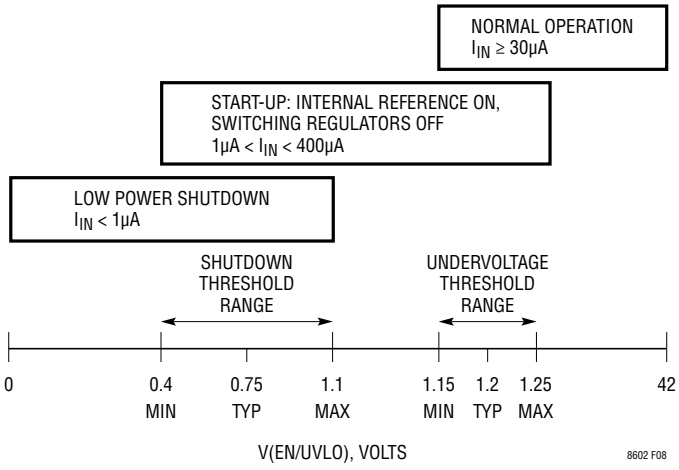


Figure 8. EN/UVLO Thresholds

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 9 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT8602's PV_{IN} pins, GND pins, and the input capacitors. The loop formed by the input capacitor should be as small as possible by placing the capacitor close to the PV_{IN} pin and the adjacent GND pin. When using a physically large input capacitor the resulting loop may become too large in which case using a small case/value capacitor placed close to the PV_{IN} and GND pins plus a larger capacitor further away is preferred. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BOOST nodes should be as small as possible. Finally, keep the FB and RT nodes small so that the ground traces will shield them from the SW and BOOST nodes. The exposed pad on the bottom of the package must be soldered to ground so that there is a good electrical connection as well as a good thermal connection so that the PCB can act as a heat sink. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under

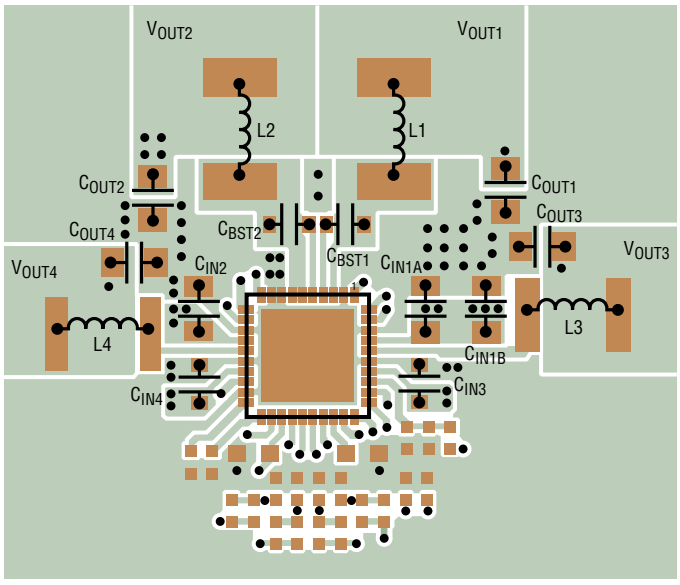


Figure 9. Recommended QFN Package PCB Layout

APPLICATIONS INFORMATION

and near the LT8602 to additional ground planes within the circuit board and on the bottom side.

Thermal Considerations

Care should be taken in the layout of the PCB to ensure good heat sinking of the LT8602. The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT8602. Recommended layer use for a 4 layer board is:

Layer 1 (Components): use 2oz copper; unbroken high frequency/high current routing (C_{IN} loop, SW node, BST node, inductor, C_{OUT}), high current DC routing, ground plane on remainder

Layer 2 (Internal): Unbroken ground plane

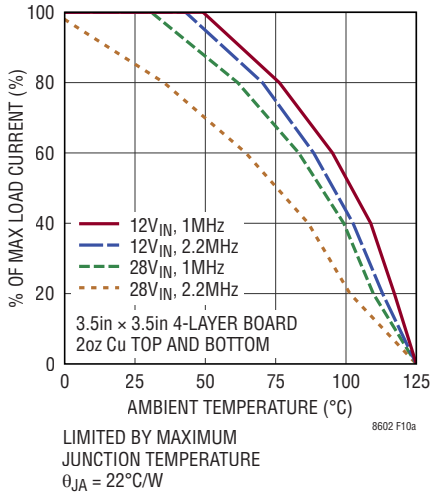
Layer 3 (Internal): Signal routing, ground plane on remainder

Layer 4 (Bottom): Use 2oz copper; high current DC routing (V_{IN}, V_{OUT}), ground plane on remainder

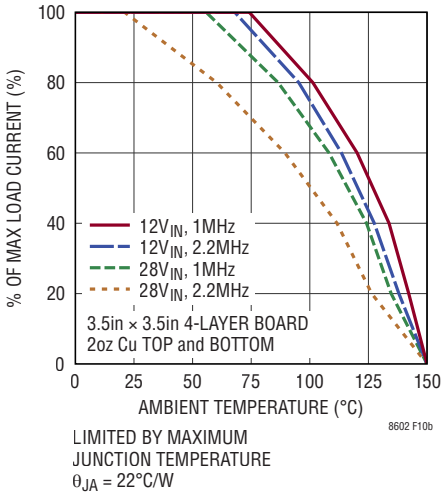
Placing additional vias can reduce thermal resistance further. Many small thermal vias are better than a few large ones. Following these PCB design guidelines can reduce the QFN θ_{JA} to 22°C/W.

Power dissipation within the LT8602 can be estimated by adding the power dissipated in each channel. Calculate each channel's power loss from an efficiency measurement and subtract the inductor loss. The die temperature is calculated by multiplying the total LT8602 power dissipation by the thermal resistance from junction to ambient and adding the ambient temperature. The maximum load current should be derated as the die temperature approaches the maximum junction rating. The LT8602 will stop switching if the internal temperature rises too high. This thermal protection is above the maximum operating temperature and is intended as a failsafe only.

Even with the best thermal practices, the LT8602 must be derated at high ambient temperature. The thermal derating curves in Figure 10 show the front page application (Ch1: $5V_{OUT}$, Ch 2: $3.3V_{OUT}$, Ch 3:$1.8V_{OUT}$, Ch 4:$1.2V_{OUT}$). The PCB layout is as described above and the θ_{JA} is 22°C/W. The output currents are decreased uniformly as a percentage of maximum. Although derating is application dependent, this set of curves is representative of typical applications with a range of frequencies and input voltages.



(10a) E- and I-Grade

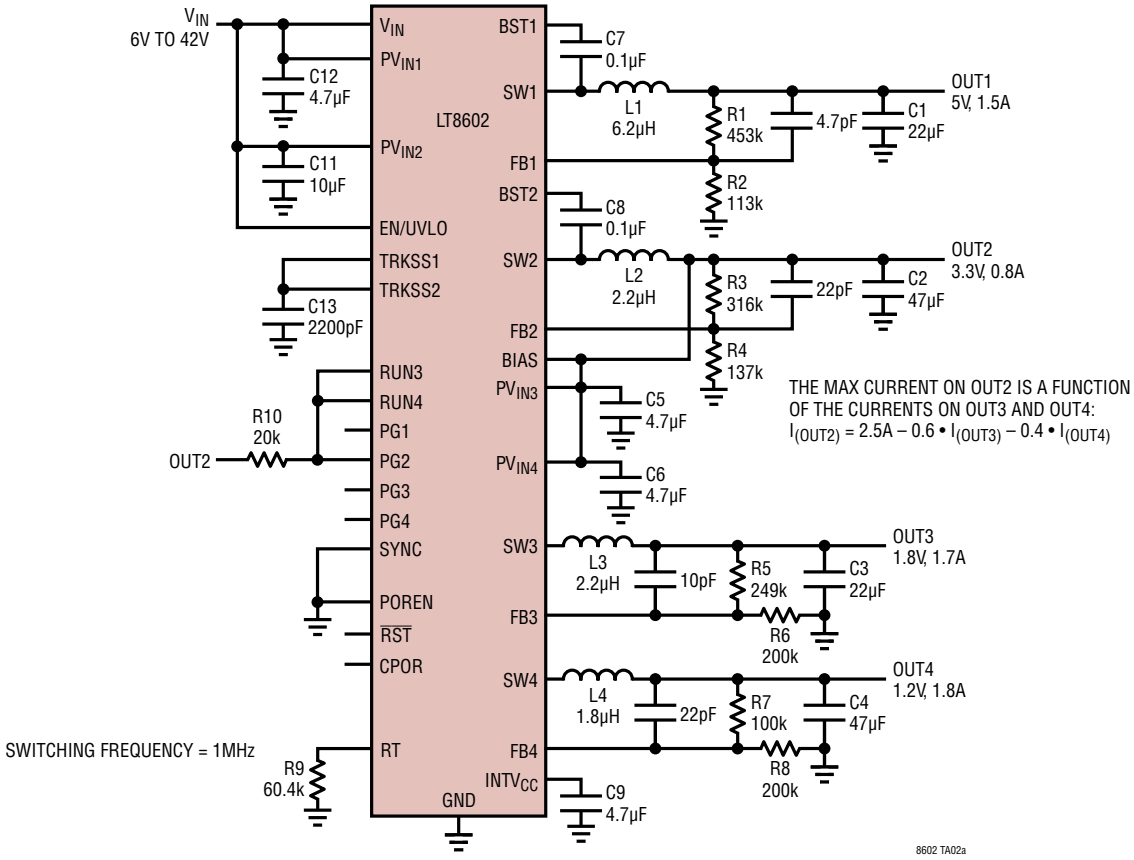


(10b) J-Grade

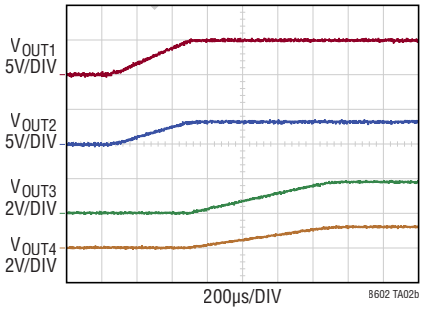
Figure 10. Thermal Derating, E-, I-, and J-Grade

TYPICAL APPLICATIONS

Details of Front Page Application



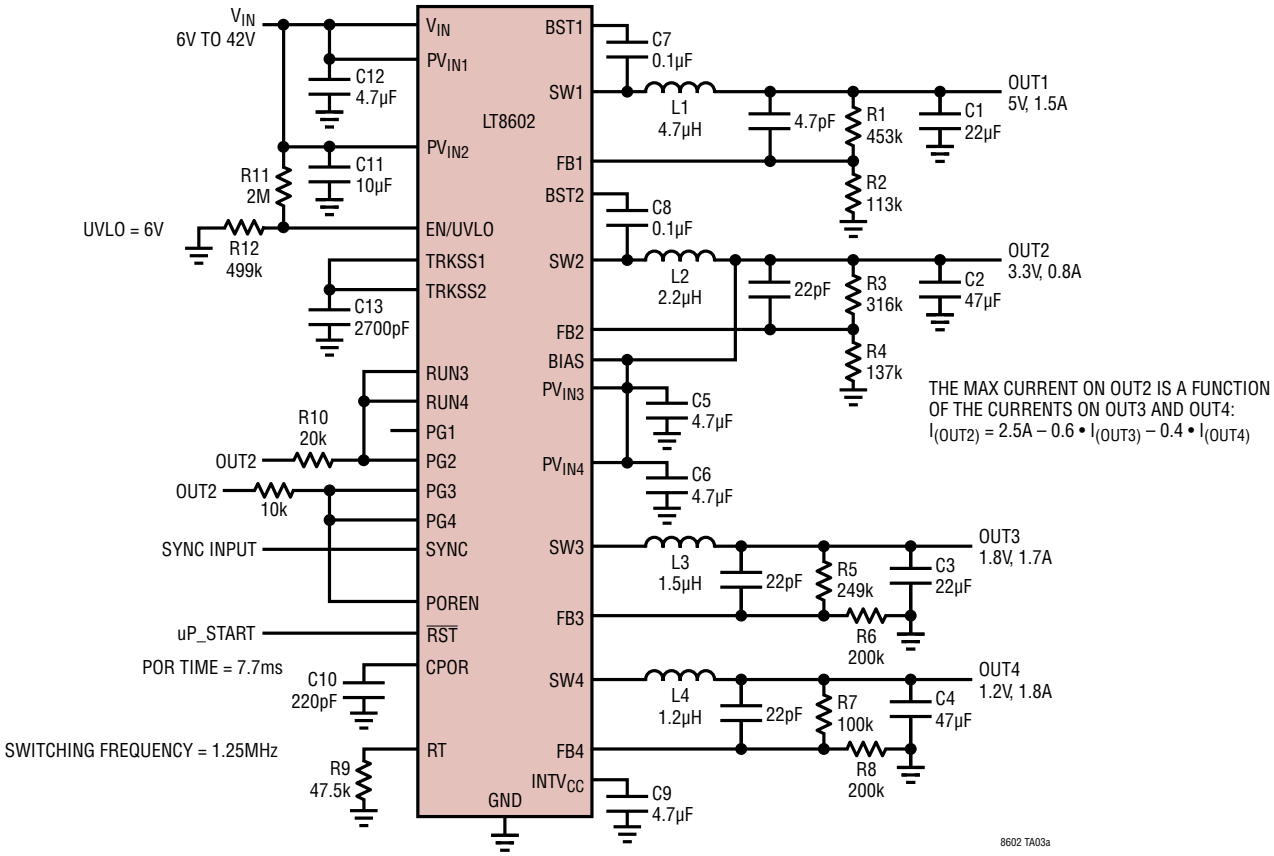
Start-Up Sequence



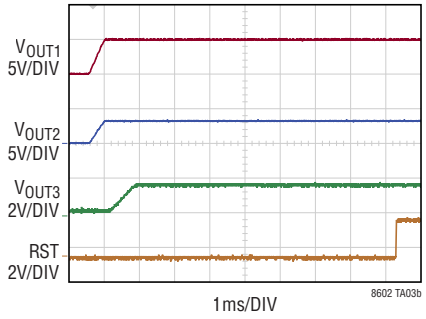
THE VALUES SHOWN ARE FOR 1MHz OPERATION.
FOR 2MHz OPERATION, MAKE THE FOLLOWING CHANGES:
L1 = 3.3µH
L2 = 1.2µH
L3 = 1.2µH
L4 = 1µH
R9 = 28.9k
THE INPUT VOLTAGE RANGE AT 2MHz IS 6V TO 24V.
ABOVE 24V, THE HV CHANNELS WILL REGULATE
BUT WITH HIGH RIPPLE DUE TO MISSED PULSES.

TYPICAL APPLICATIONS

Automotive Input Steps Down to 5V, 3.3V, 1.8V and 1.2V



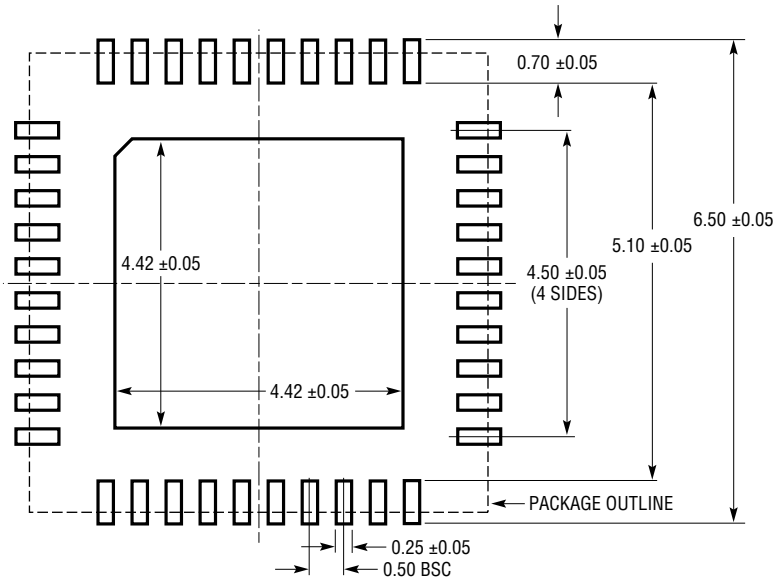
Start-Up Sequence



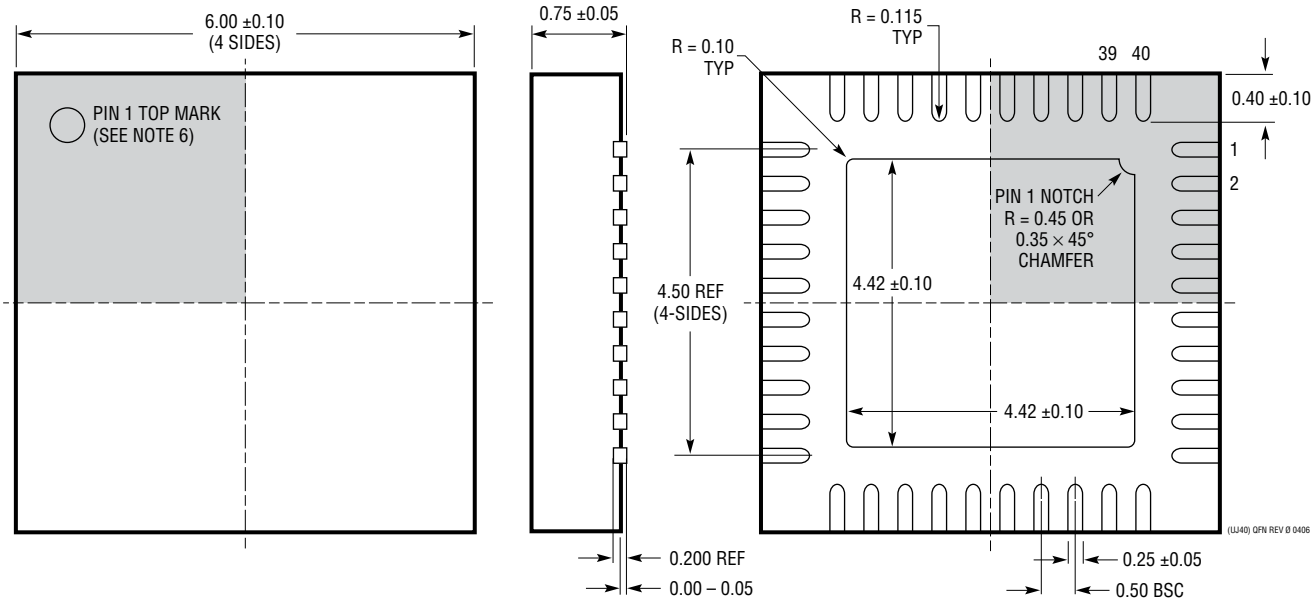
START-UP SEQUENCE:
CH1 AND CH2 SOFT-START
RATIOMETRICALLY;
THEN CH3 AND CH4 TURN ON;
THEN POR TIMER STARTS.

PACKAGE DESCRIPTION

UJ Package
40-Lead Plastic QFN (6mm × 6mm)
(Reference LTC DWG # 05-08-1728 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

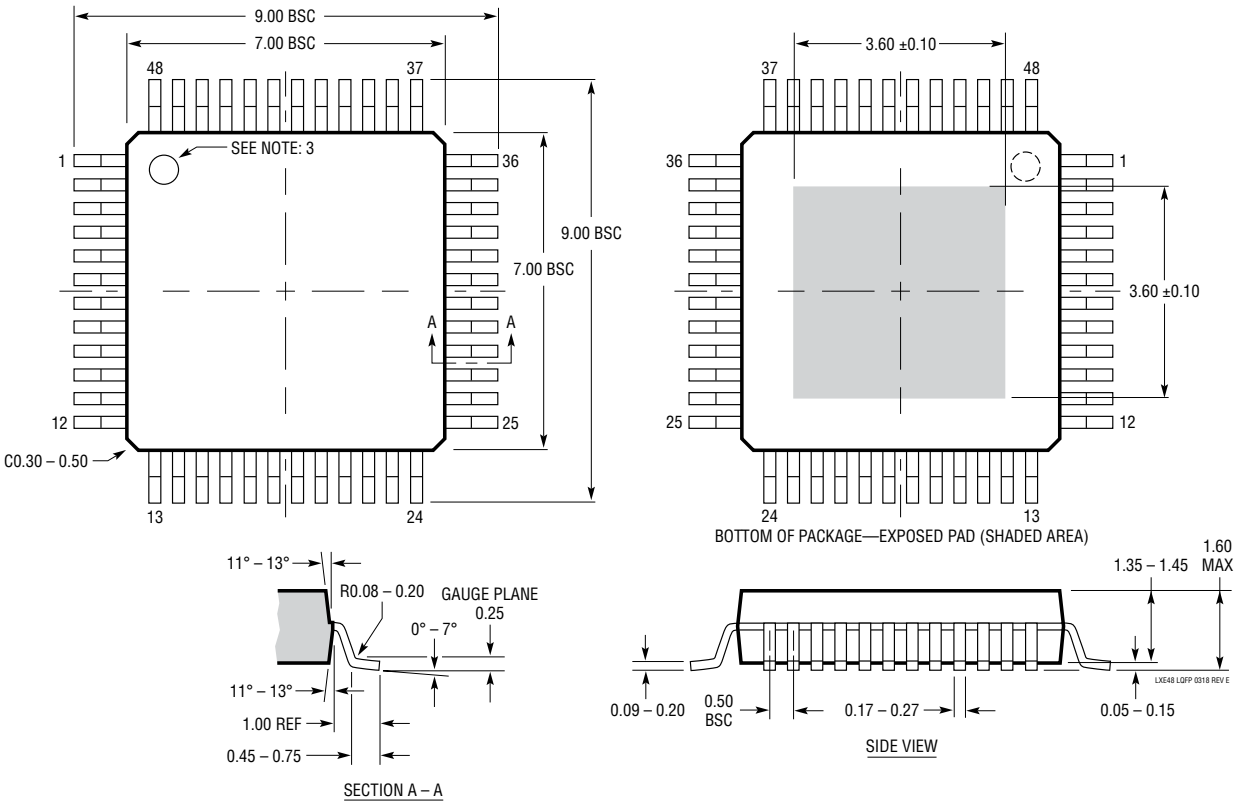


BOTTOM VIEW—EXPOSED PAD

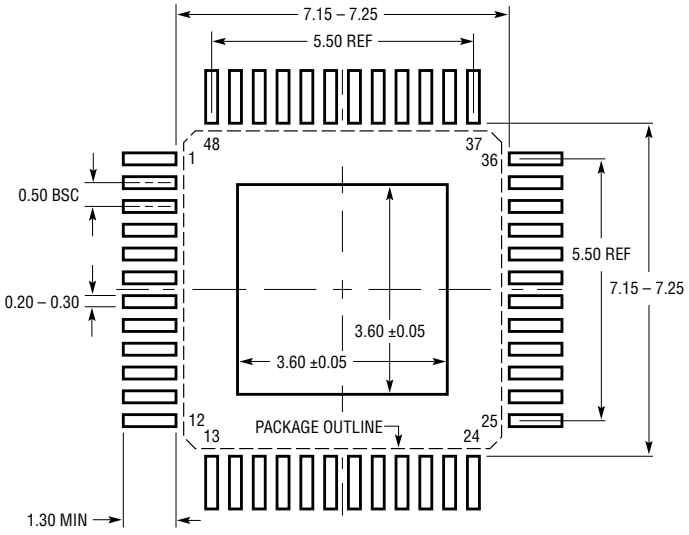
NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

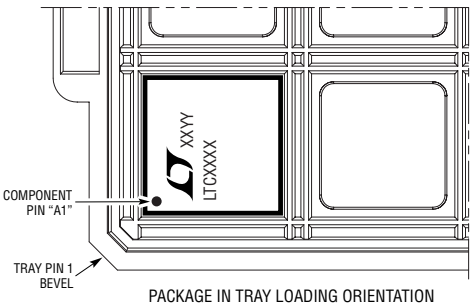
PACKAGE DESCRIPTION

LXE Package
48-Lead Plastic Exposed Pad LQFP (7mm × 7mm)
(Reference LTC DWG #05-08-1832 Rev E)
Exposed Pad Variation BB



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.25mm (10 MILS) BETWEEN THE LEADS AND ON ANY SIDE OF EXPOSED PAD, MAX 0.50mm (20 MILS) AT CORNER OF EXPOSED PAD, IF PRESENT
3. PIN-1 INDENTIFIER IS A MOLDED INDENTATION
4. DRAWING IS NOT TO SCALE





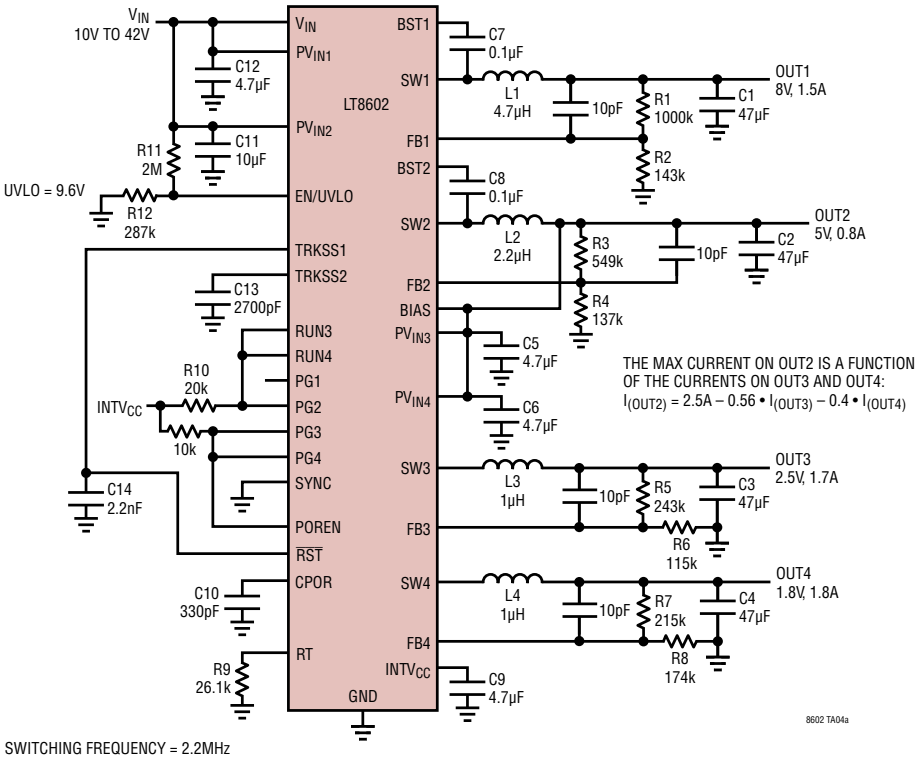
Rev. C

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/16	Revised Electrical Characteristics tables and temperature dotted soft-start.	4, 5
		Replaced G06 and G07 curves.	6
		Revised Pin Functions for BIAS, EN/UVLO $INTV_{CC}$.	11
		Changed Figure 7.	20
B	06/17	Added LQFP package option.	1,2
		Added Pin Functions for LQFP package option.	11,12
		Clarified Figure 9 for QFN package.	22
		Added clarified drawing for front page application.	25
		Typical Application moved from page 25 to 26.	26
		Clarified QFN package drawing.	27
		Added LQFP package option.	28
C	12/20	Added AEC-Q100 Qualified statement.	1
		Add J-Grade and Automotive products to Order Information table.	2
		Add J-Grade spec to Electrical Characteristics table, clarified condition. Clarified Note 2 J-Grade.	3, 4, 5
		Clarified Input/Output Capacitor Selection for J-Grade.	18, 19
		Add Thermal Derating graph for J-Grade.	24

TYPICAL APPLICATION

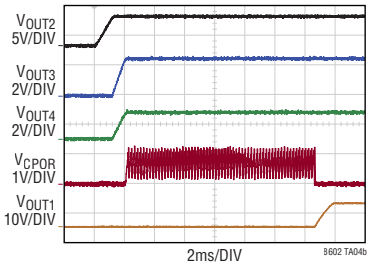
10V to 42V Input Steps Down to 5V, 2.5V, 1.8V and 8V (Delayed)



THE MAX CURRENT ON OUT2 IS A FUNCTION OF THE CURRENTS ON OUT3 AND OUT4:
$I_{(OUT2)} = 2.5A - 0.56 \bullet I_{(OUT3)} - 0.4 \bullet I_{(OUT4)}$

SWITCHING FREQUENCY = 2.2MHz

Start-Up Sequence



IN THIS APPLICATION, THE POR IS USED AS A DELAY FOR THE 8V SUPPLY. THE 8V SUPPLY WILL START RAMPING UP 12ms AFTER ALL OTHER SUPPLIES HAVE REACHED REGULATION.

START-UP SEQUENCE:
CH2 SOFT-STARTS;
THEN CH3 AND CH4 TURN ON;
THEN POR TIMER STARTS;
AFTER POR TIMES OUT, THEN CH1 SOFT-STARTS.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3507/ LT3507A	36V, 2.7A + 1.8A + 1.8A + LDO Controller, 2.5MHz, High Efficiency, Triple Output Step-Down DC/DC Converter	V_{IN} = 4V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 7mA, I_{SD} < 1µA, 5mm × 7mm QFN
LT8640	42V, 6A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 4mm QFN
LT8616	42V Dual (2.5A + 1.5A), 95% Efficiency 3MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 6.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 6.5µA, I_{SD} < 1µA, TSSOP-28E Package
LT8614	42V, 4A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 4mm QFN
LT8612	42V, 6A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 6mm QFN
LT8610	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E
LT8611	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA and Input/Output Current Limit/Monitor	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V , I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 5mm QFN-24
LT8610A/ LT8610AB	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 3.4V to 42V, $V_{OUT(MIN)}$ = 0.985V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E